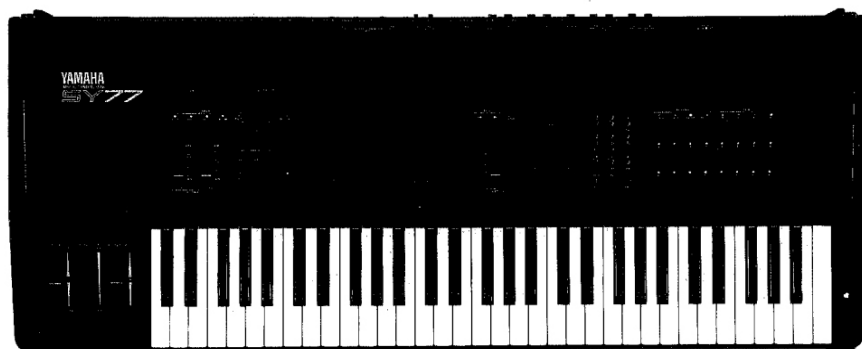


MUSIC SYNTHESIZER

SY77

SERVICE MANUAL

SY77



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IMPORTANT NOTICE

This manual has been provided for the use of authorized Yamaha Retailers and their service personnel. It has been assumed that basic service procedures inherent to the industry, and more specifically Yamaha Products, are already known and understood by the users, and have therefore not been restated.

WARNING: Failure to follow appropriate service and safety procedures when servicing this product may result in personal injury, destruction of expensive components and failure of the product to perform as specified. For these reasons, we advise all Yamaha product owners that all service required should be performed by an authorized Yamaha Retailer or the appointed service representative.

IMPORTANT: The presentation or sale of this manual to any individual or firm does not constitute authorization, certification, recognition of any applicable technical capabilities, or establish a principle-agent relationship of any form.

The data provided is believed to be accurate and applicable to the unit(s) indicated on the cover. The research, engineering, and service departments of Yamaha are continually striving to improve Yamaha products. Modifications are, therefore, inevitable and changes in specification are subject to change without notice or obligation to retrofit. Should any discrepancy appear to exist, please contact the distributor's Service Division.

WARNING: Static discharges can destroy expensive components. Discharge any static electricity your body may have accumulated by grounding yourself to the ground buss in the unit (heavy gauge black wires connect to this buss).

IMPORTANT: Turn the unit **OFF** during disassembly and parts replacement. Recheck all work before you apply power to the unit.

This product uses a lithium battery for memory back-up.

WARNING: Lithium batteries are dangerous because they can be exploded by improper handling. Observe the following precautions when handling or replacing lithium batteries.

- Leave lithium battery replacement to qualified service personnel.
- Always replace with batteries of the same type.
- When installing on the PC board, solder using the connection terminals provided on the battery cells. Never solder directly to the cells. Perform the soldering as quickly as possible.
- Never reverse the battery polarities when installing.
- Do not short the batteries.
- Do not attempt to recharge these batteries.
- Do not disassemble the batteries.
- Never heat batteries or throw them into fire.

ADVARSEL!

Lithiumbatteri. Eksplosionsfare.

Udskiftning må kun foretages af en sagkyndig, og som beskrevet i servicemanualen.

■ SPECIFICATIONS

- **Tone generator:** Realtime Convolution and Modulation (RCM)
AWM2: 16 bit linear waveform data, maximum 48k Hz sampling frequency
AFM: 6 operators, 45 algorithms, 3 feedback loops, 16 waveforms, modulation from AWM output
Filter: Time variant IIR (infinite impulse response) digital filters, 2 filters for each element (maximum of 8 filters per voice)
Maximum simultaneous notes: 16 notes AWM + 16 notes AFM
Maximum simultaneous timbres: 16
Note assignment: Last note priority, DVA (dynamic voice allocation)
- **Keyboard:** 61 notes, key velocity sensitivity, channel aftertouch
- **DSP effects:** (reverb effect+modulation effect) × 2
Reverb effects: 40 types
Modulation effects: 4 types
- **Sequencer:** Tracks: 16 (15 tracks+1 pattern track)
Songs: 1
Resolution: 1/96 of a quarter note (for internal clock)
Maximum simultaneous notes: 32
Capacity: approximately 16,000 notes
Patterns: 99
Recording: realtime/step/punch in
- **Memory:** Preset memory: 128 voices, 16 multis
Internal memory: 64 voices, 16 multis
Waveform memory: 2 Mwords (4 Mbytes), 112 sounds
Card slots: synthesizer data × 1, waveform data × 1
Disk: 3.5" floppy disk drive (713K byte formatted)
- **Controllers:** Wheels: PITCH, MODULATION 1, MODULATION 2
Slider: OUTPUT 1, OUTPUT 2, DATA ENTRY
Knobs: LCD contrast, click volume
Dial: data entry dial
Panel switches: MODE × 5, EDIT/COMPARE, COPY/SAVE, EF.BYPASS, SEQUENCER × 7, SHIFT, function × 8, EXIT, PAGE < >, JUMP/MARK, cursor Δ ∇ < >, -1/NO, +1/YES, numeric keypad 0-9, MEMORY × 4, BANK × 4, voice select × 16
- **Display:** LCD: 240 × 64 pixels (backlit)
LED: red × 11, red/green × 21
- **Terminals:** Audio output: OUTPUT 1 (L/MIX, L/MONO, R/MIX R), OUTPUT 2 (L, R), PHONES Controller: BREATH, FOOT VOLUME, FOOT CONTROLLER, SUSTAIN, FOOT SWITCH
MIDI: IN, OUT, THRU
- **Power requirements:** U.S. & Canadian models: 120V
European & Australian models: 220-240V
- **Power consumption:** U.S. & Canadian models: 28W
European & Australian models: 28W
- **Dimensions:** 1046 (W) × 407 (D) × 119 (H) mm
- **Weight:** 17kg
- **Output level:** Headphones: -1dBm
Output terminals: -10dBm
- **Accessory:** Floppy disk (3.5 inch) × 1
Plug cover × 1

■ 総合仕様

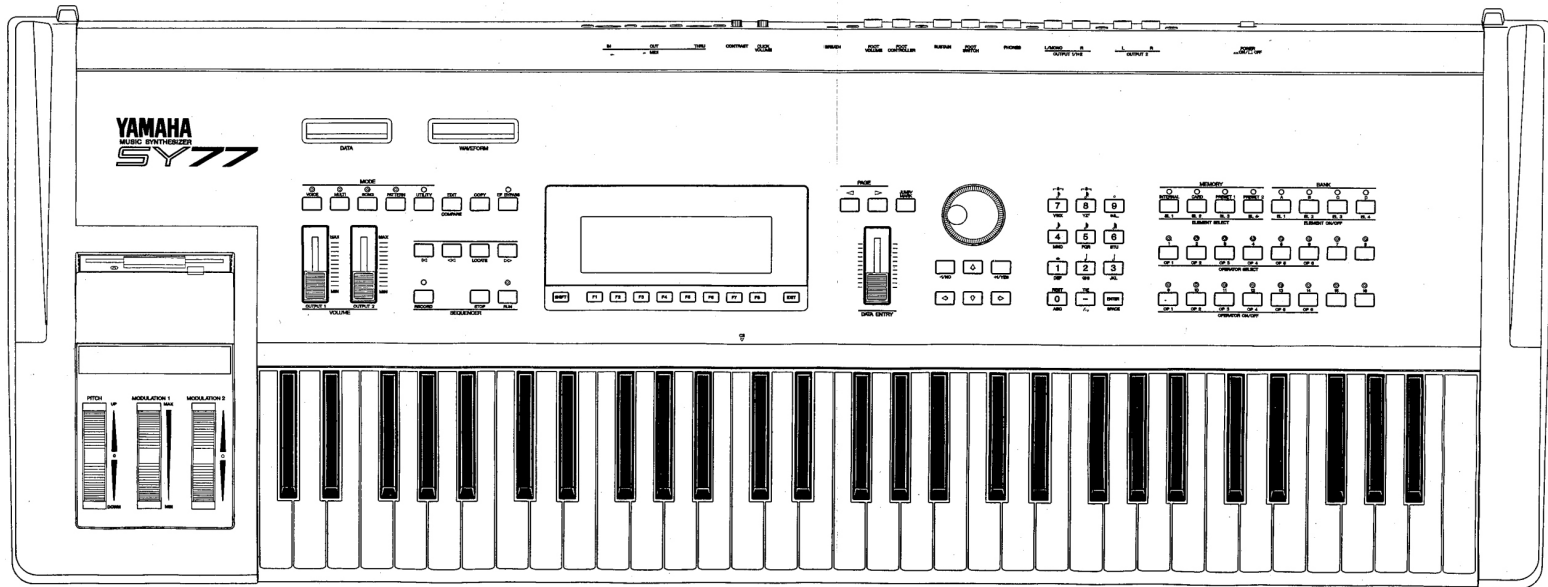
- 音源
 - 音源形式 : RCM音源
(Realtime Convolution and Modulation)
 - AWM2 : 16ビットリニア波形、サンプリング周波数最大48kHz
1音(エレメント)につき1オクターブ 12dBのデジタルフィルターを2個搭載
 - AFM : 6オペレータ、45アルゴリズム、3系統フィードバック、16波形
AWM2の出力波形による変調が可能
1音(エレメント)につき1オクターブ 12dBのデジタルフィルターを2個搭載
- フィルター : 時変形デジタルフィルター×最大8/ボックス
: 各フィルターはLPF,HPFの切り替えができ、この組合せによりBPFやロールオフ24dBのLPFとしても使用可能
: レゾナンス可変で発振領域までカバー
- 最大同時発音数 : AWM2 : 16音 + AFM : 16音
- 最大同時音色数 : 16
- 発音形式 : 後着優先、DVA
- 鍵盤 : 61キー/イニシャル&チャンネルアフタータッチ付き
- エフェクタータイプ : (リバーブ系+モジュレーション系)×2系統
 - リバーブ系 : 40タイプ
 - モジュレーション系 : 4タイプ
- シーケンサー
 - トラック数 : 16トラック(含むパターントラック1)
 - ソング : 1
 - 分解能 : 1/96(内部クロック時)
 - 最大同時発音数 : 32
 - 最大記憶音数 : 約16000音
 - パターン数 : 99
 - 録音方式 : リアルタイム/ステップ/パンチイン
- プリセットメモリー : ボイス : 128+マルチ : 16
- インターナルメモリー : ボイス : 64+マルチ : 16
- 波形用メモリー : 2Mワード(4Mバイト)
: 楽器音×92
: リズム×20
- カードスロット : 音色パラメータ用×1
MCD64 : 1バンク
※ 1バンク : 64ボイス+16マルチ+1システム
: 波形用×1(512Kワード)
- 3.5インチFDD : 1(フォーマット時713KB)
- Wheel : ピッチベンド、モジュレーション1、モジュレーション2
- スライダーボリューム : アウトプットボリューム1・2、データエントリー
- ロータリーボリューム : LCDコントロール、クリックボリューム
- ダイヤル : データエントリー
- パネルスイッチ
 - Mode : 5 Voice, Multi, Song, Pattern, Utility
 - Edit : 2 Edit/Compare, Copy
 - Effect bypass : 1
 - Memory select : 4 Preset 1, Preset 2, Internal, Card
 - Bank select : 4 A~D
 - Voice select : 16 1~16
 - Page : 3 Page+, Page-, Jump/Mark
 - テンキー : 12 0~9, Enter, -
 - Data Entry : 2 Inc, Dec
 - カーソル : 4 ←, →, ↑, ↓
 - Function : 10 Function 1~8, Shift, Exit
 - Sequencer : 7 Run, Stop, Rec, Top, Rew, FF, Auto, Locate
- LCD : 240×64Dots(バックライト付き)
- LED : Red×11
: Red/Green×21
- 音声出力 : 4 Output 1(L/Mix L/Mono, R/Mix R), Output 2(L,R)
- ヘッドフォン : 1
- コントローラー : 6 Foot control, Foot volume, Foot switch, Sustain switch, Breath control
- MIDI : 3 IN, OUT, THRU
- ヘッドフォン出力レベル : -1dBm
- リア出力端子レベル : -10dBm
- 電源電圧 : 100V
- 消費電力 : 20W
- 寸法 : 1046(W)×407(D)×119(H)mm
- 重量 : 17kg
- 付属品 : デモディスク1枚
(3.5インチフロッピーディスク)
: プラグカバー 1個

SY77

SY77

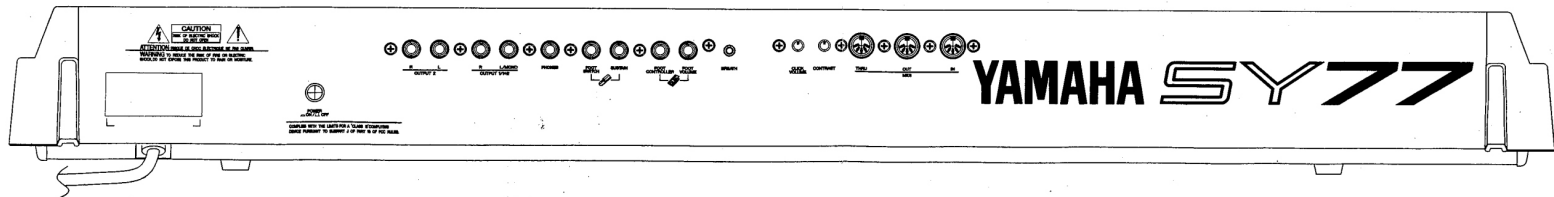
■ PANEL LAYOUT (パネルレイアウト)

● Front Panel (フロントパネル)

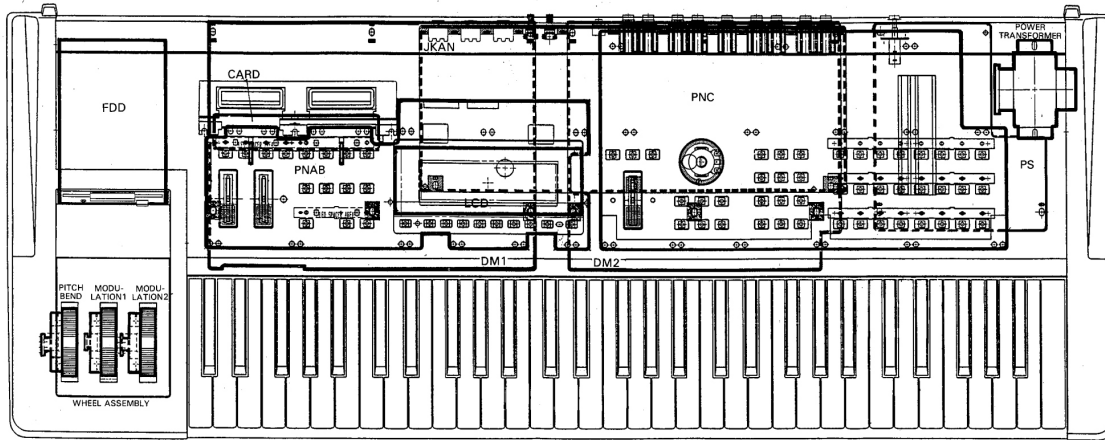


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● Rear Panel (リアパネル)

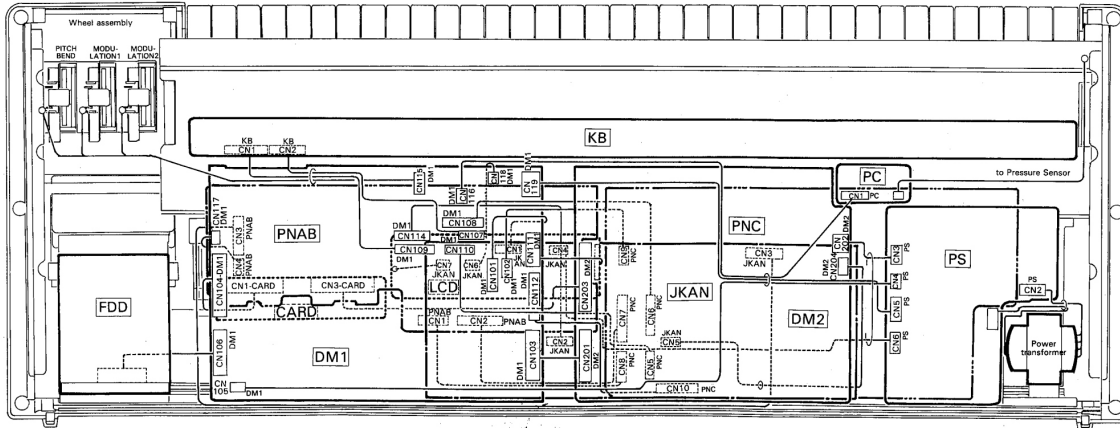


■ CIRCUIT BOARD LAYOUT (ユニットレイアウト)

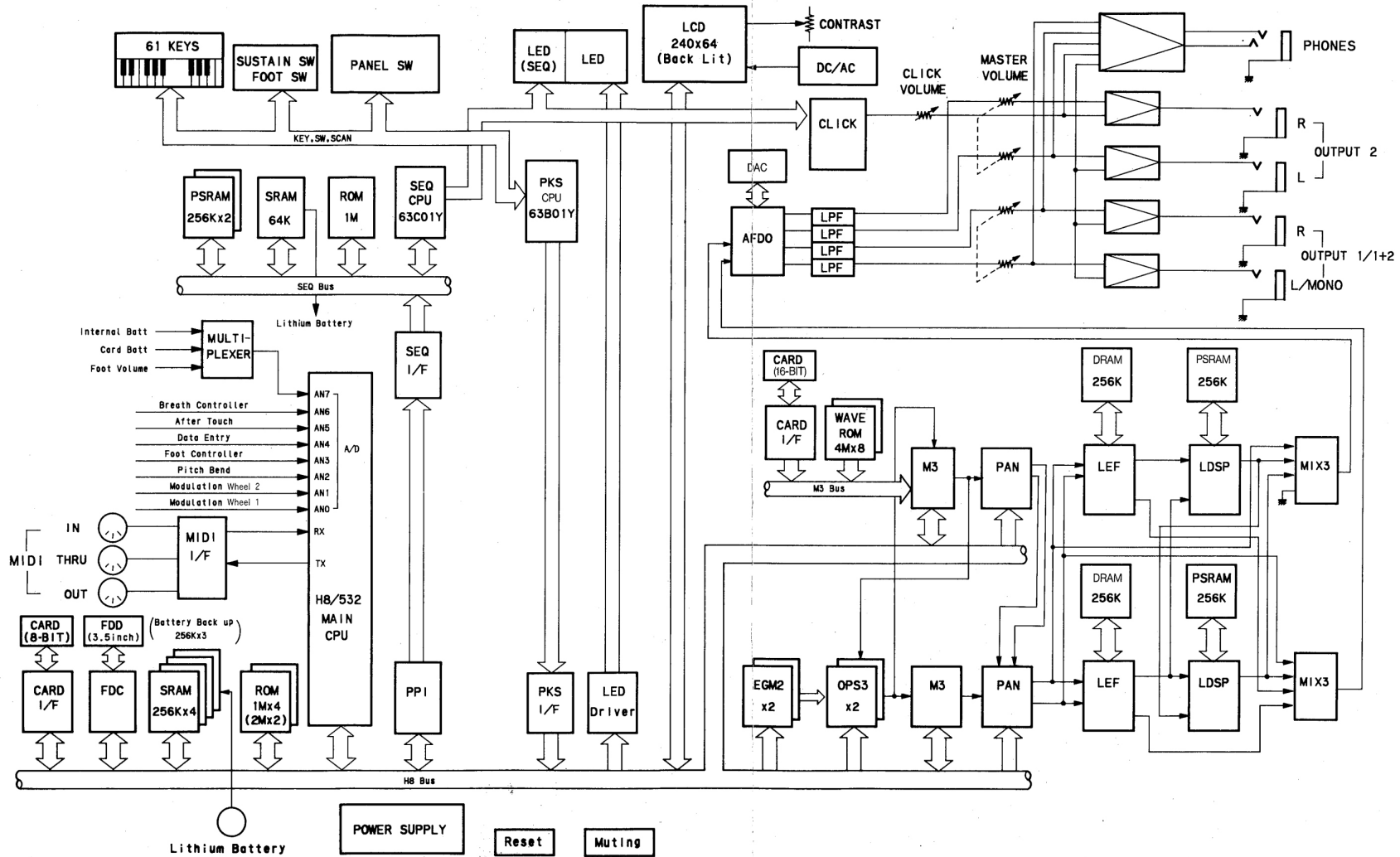


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● Wiring (配線図)



■ BLOCK DIAGRAM (ブロックダイアグラム)



SY77

■ DISASSEMBLY PROCEDURE (分解手順)

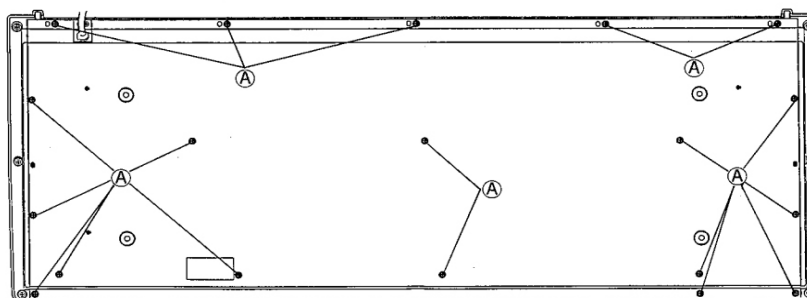
1. Bottom Cover Assembly (refer to fig. 1.)

1-1. Remove the nineteen (19) screws ① (4.0×10 bonding head tapping screw), the Bottom cover assembly can be removed.

This will give you access to the DM1, DM2, PS circuit boards, Floppy disk drive unit and Wheel assembly.

1. 底板 Ass'y の外し方 (図 1 参照)

1-1. ①のネジ19本(4×10ボンディングBタイトネジ)を外して取り外します。



(fig. 1)

2. DM1 Circuit Board (refer to fig.2)

2-1. Remove the Bottom cover assembly. (see procedure 1.)

2-2. Remove the six (6) screws ② (4.0×10 bind head tapping screw), the DM1 circuit board can be raised.

After the connectors have been disconnected, the DM1 circuit board can be taken out of the unit completely.

2. DM1 シートの外し方 (図 2 参照)

2-1. 底板 Ass'y を外します。(1項参照)

2-2. ②のネジ6本(4×10バインドタッピングネジ)と束線を外して取り外します。

3. DM2 Circuit Board (refer to fig.2)

3-1. Remove the Bottom cover assembly. (see procedure 1.)

3-2. Remove the six (6) screws ③ (4.0×10 bind head tapping screw), the DM2 circuit board can be raised.

After the connectors have been disconnected, the DM2 circuit board can be taken out of the unit completely.

3. DM2 シートの外し方 (図 2 参照)

3-1. 底板 Ass'y を外します。(1項参照)

3-2. ③のネジ6本(4×10バインドタッピングネジ)と、束線を外して取り外します。

4. PS Circuit Board (refer to fig. 2.)

4-1. Remove the Bottom cover assembly. (see procedure 1.)

4-2. Remove the screw ④ (4.0×10 bonding head tapping screw) to remove the AC panel.

4-3. The PS circuit board can be removed by removing the four (4) screws ⑤ (4.0×10 bind head tapping screw) and disconnecting the connectors.

4. PS シートの外し方 (図 2 参照)

4-1. 底板 Ass'y を外します。(1項参照)

4-2. ④のネジ1本(4×10ボンディングBタイトネジ)を外し、ACパネルを外しておきます。

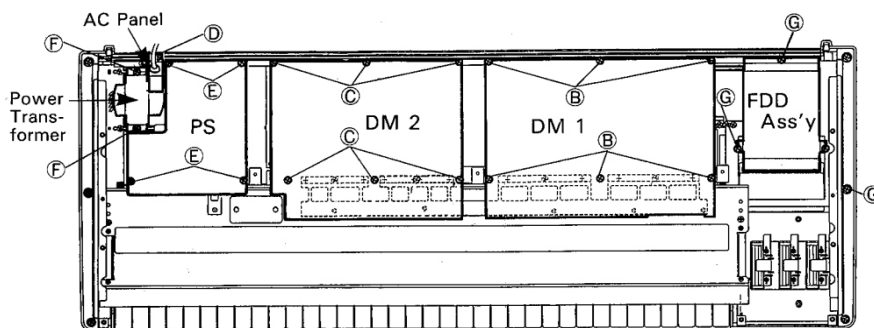
4-3. ⑤のネジ4本(4×10バインドタッピングネジ)と、束線を外して取り外します。

5. Power Transformer (refer to fig. 2.)

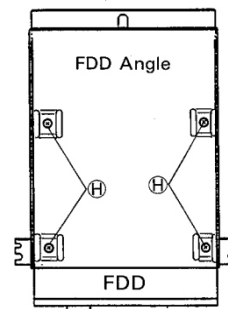
- 5-1. Remove the Bottom cover assembly. (see procedure 1.)
- 5-2. Remove the PS circuit board. (see procedure 4.)
- 5-3. Remove the two (2) screws ⑥ (4.0×10 bind head tapping screw) to remove the Power transformer.

6. Floppy Disk Drive Unit (refer to fig.2 and fig. 3)

- 6-1. Remove the Bottom cover assembly. (see procedure 1.)
- 6-2. Remove the three (3) screws ③ (4.0×10 bind head tapping screw) and disconnect the connectors, the Floppy disk drive unit can be taken out of the SY77 unit.
- 6-3. To remove the FDD holder from the Floppy disk drive unit, remove the four (4) screws ④ (3.0×6 bind head tapping screw).



(fig. 2)



(fig. 3)

5. 電源トランスの外し方 (図2参照)

- 5-1. 底板Ass'yを外します。(1項参照)
- 5-2. PSシートを外します。(4項参照)
- 5-3. ⑥のネジ2本(4×10バインドタッピングネジ)を外します。

6. FDDの外し方 (図2, 3参照)

- 6-1. 底板Ass'yを外します。(1項参照)
- 6-2. ③のネジ3本(4×10バインドタッピングネジ)と束線を外して、FDD Ass'yを取り外します。FDD金具は④のネジ4本(3×6バインド小ネジ)を外して取り外します。

7. CARD Circuit Board (refer to fig. 4)

- 7-1. Remove the Bottom cover assembly. (see procedure 1.)
- 7-2. Remove the DM1 circuit board. (see procedure 2.)
- 7-3. After the three (3) screws ① (4.0×10 bind head tapping screw) have been removed, the CARD circuit board can be removed.

8. JKAN Circuit Board (refer to fig. 4 and fig. 5)

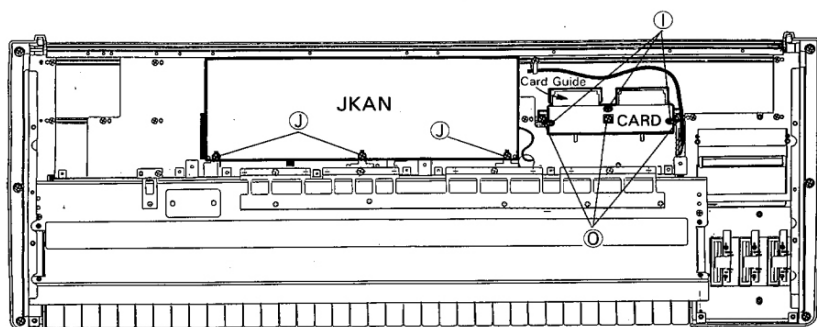
- 8-1. Remove the Bottom cover assembly. (see procedure 1.)
- 8-2. Remove the DM1 and DM2 circuit boards. (see procedures 2 and 3.)
- 8-3. Remove the ten (10) screws ⑫ (4.0×10 bonding head tapping screw) on the rear panel and three (3) screws ① (4.0×10 bind head tapping screw), the JKAN circuit board can be removed.

7. CARDシートの外し方 (図4参照)

- 7-1. 底板Ass'yを外します。(1項参照)
- 7-2. DM1シートを外します。(2項参照)
- 7-3. ①のネジ3本(4×10バインドタッピングネジ)と、束線を外して取り外します。

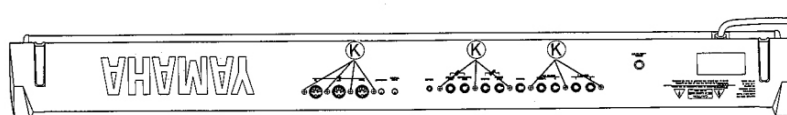
8. JKANシートの外し方 (図4, 5参照)

- 8-1. 底板Ass'yを外します。(1項参照)
- 8-2. DM1シートとDM2シートを外します。
(2と3項参照)
- 8-3. ①のネジ3本(4×10バインドタッピングネジ)と、リアパネル側より止めている⑫のネジ10本(4×10ボンディングBタイトネジ)と、束線を外して取り外します。



(fig. 4)

• Rear View



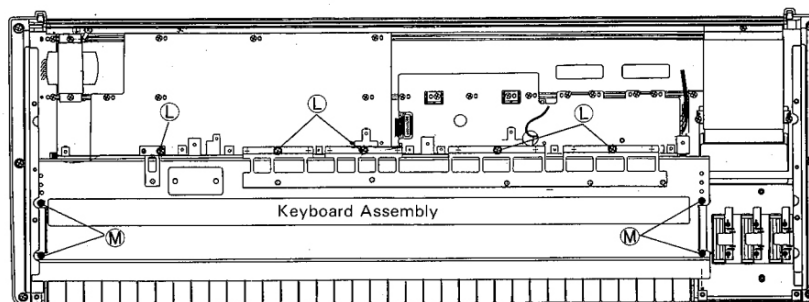
(fig. 5)

9. Keyboard Assembly (refer to fig. 6.)

- 9-1. Remove the Bottom cover assembly. (see procedure 1.)
- 9-2. Remove the DM1 and DM2 circuit boards. (see procedures 2 and 3.)
- 9-3. Remove the PS circuit board. (see procedure 4.)
- 9-4. The Keyboard assembly can be removed by removing the five (5) screws ① (4.0 × 10 bind head tapping screw) and four (4) screws ② (4.0 × 16 bind head tapping screw).

9. 鍵盤Ass'yの外し方 (図6参照)

- 9-1. 底板Ass'yを外します。(1項参照)
- 9-2. DM1シートとDM2シートを外します。
(2と3項参照)
- 9-3. PSシートを外します。(4項参照)
- 9-4. ①のネジ5本(4×10バインドタッピングネジ)と②のネジ4本(4×16バインドタッピングネジ)を外して取り外します。



(fig. 6)

10. PNAB and PNC Circuit Boards (refer to fig. 4 and fig. 7)

- 10-1. Pull out the knobs on the Control panel.
- 10-2. Remove the Bottom cover assembly. (see procedure 1.)
- 10-3. Remove the DM1 and DM2 circuit boards. (see procedures 2 and 3.)
- 10-4. Remove the PS circuit board. (see procedure 4.)
- 10-5. Remove the JKAN circuit board. (see procedure 8.)
- 10-6. Remove the Keyboard assembly. (see procedure 9.)
- 10-7. Remove the fourteen (14) screws ③ (4.0 × 10 bind head tapping screw) to remove the Center angle bracket.

10. PNABシートとPNCシートの外し方 (図4, 7参照)

- 10-1. パネル表側より、スライドボリューム類のつまみを抜きとっておきます。
- 10-2. 底板Ass'yを外します。(1項参照)
- 10-3. DM1シートとDM2シートを外します。
(2と3項参照)
- 10-4. PSシートを外します。(4項参照)
- 10-5. JKANシートを外します。(8項参照)
- 10-6. 鍵盤Ass'yを外します。(9項参照)
- 10-7. ③のネジ14本(4×10バインドタッピングネジ)を外して、センターアングルを取り外します。

10-8. PNAB circuit board removal

10-8-1. Remove the CARD circuit board. (see procedure 6.)

10-8-2. Remove the three (3) screws ㉑ (4.0×10 bind head tapping screw) to remove the Card guide.

10-8-3. After the seven (7) screws ㉒ (4.0×10 bind head tapping screw) have been removed, the PNAB circuit board can be removed.

* The PNAB circuit board is connected to the PNC circuit board with wire harnesses.

10-9. PNC circuit board removal

10-9-1. After the eight (8) screws ㉓ (4.0×10 bind head tapping screw) have been removed, the PNC circuit board can be removed.

10-8. PNABシートの外し方

10-8-1. CARDシートを外します。(6項参照)

10-8-2. ㉑のネジ3本(4×10バインドタッピングネジ)を外してカードガイドを取り外します。

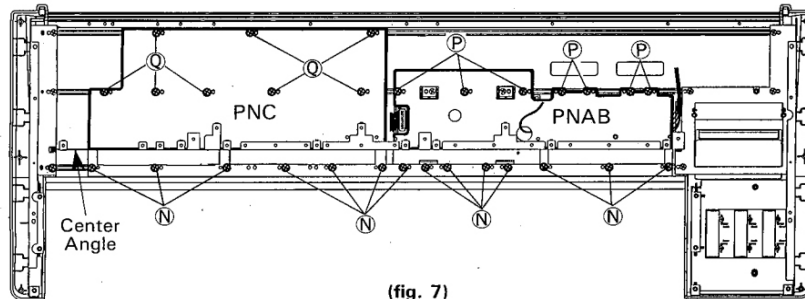
10-8-3. ㉒のネジ7本(4×10バインドタッピングネジ)を外せばPNABシートが外れます。

※束線も一緒に外す場合は、PNCシートも外して行って下さい。

10-9. PNCシートの外し方

10-9-1. ㉓のネジ8本(4×10バインドタッピングネジ)を外して取り外します。

※束線も一緒に外す場合は、PNABシートも外して行って下さい。



(fig. 7)

11. LCD Circuit Board (refer to fig. 8)

11-1. Remove the Bottom cover assembly. (see procedure 1.)

11-2. Remove the DM1 and DM2 circuit boards. (see procedures 2 and 3.)

11-3. Remove the PS circuit board. (see procedure 4.)

11-4. Remove the JKAN circuit board. (see procedure 8.)

11-5. Remove the Keyboard assembly. (see procedure 9.)

11-6. Remove the PNAB circuit board. (see procedure 10.)

11-7. The LCD circuit board can be removed by removing the four (4) screws ㉔ (3.0×8 bind head tapping screw).

11. LCDシートの外し方 (図8参照)

11-1. 底板Ass'yを外します。(1項参照)

11-2. DM1とDM2シートを外します。(2と3項参照)

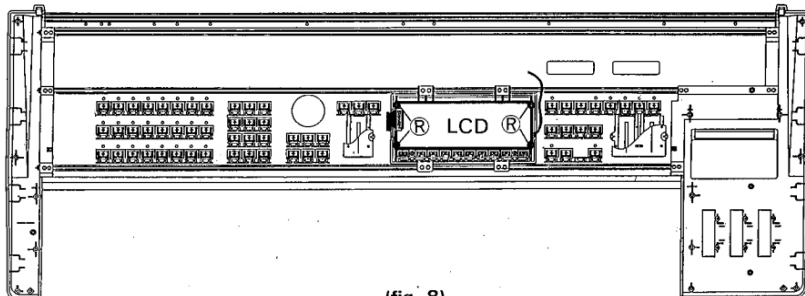
11-3. PSシートを外します。(4項参照)

11-4. JKANシートを外します。(8項参照)

11-5. 鍵盤Ass'yを外します。(9項参照)

11-6. PNABシートを外します。(10項参照)

11-7. ㉔のネジ4本(3×8バインドタッピングネジ)を外せばLCDシートが外れます。



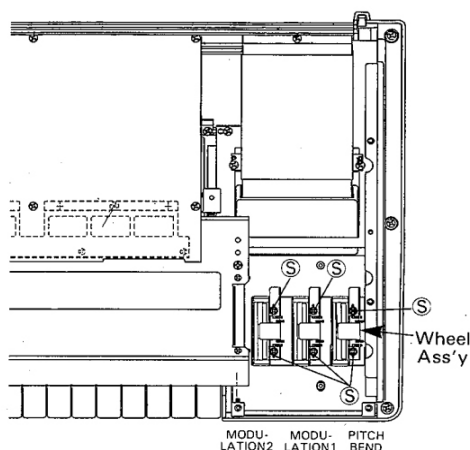
(fig. 8)

12. Wheel Assembly (refer to fig. 9)

- 12-1. Remove the Bottom cover assembly. (see procedure 1.)
- 12-2. After the six (6) screws ⑤ (3.0 × 8 bonding head tapping screw) have been removed, the Wheel assembly can be removed.

12. ホイールAss'yの外し方 (図9参照)

- 12-1. 底板を外します。
- 12-2. ⑤のネジ6本(3 × 8 ボンディングBタイトネジ)と束線を外して取り外します。



(fig. 9)

13. Rotary Encoder Knob (Data Entry)

- 13-1. Remove the Bottom cover assembly. (see procedure 1.)
- 13-2. Remove the DM1 and DM2 circuit boards. (see procedures 2 and 3.)
- 13-3. Remove the PS circuit board. (see procedure 4.)
- 13-4. Remove the JKAN circuit board. (see procedure 8.)
- 13-5. Remove the Keyboard assembly. (see procedure 9.)
- 13-6. Remove the PNC circuit board. (see procedure 10.)
- 13-7. Pull out the Rotary encoder knob on the PNC circuit board.

13. ロータリーエンコーダツマミ(データエントリー)の外し方

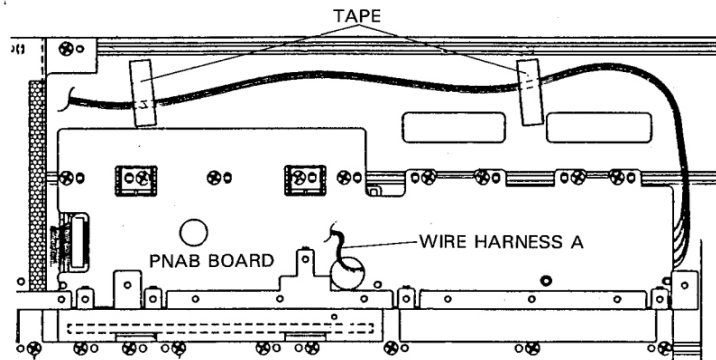
- 13-1. 底板Ass'yを外します。(1項参照)
- 13-2. DM1 とDM2 シートを外します。(2と3項参照)
- 13-3. PSシートを外します。(4項参照)
- 13-4. JKANシートを外します。(8項参照)
- 13-5. 鍵盤 Ass'yを外します。(9項参照)
- 13-6. PNCシートを外します。(10項参照)
- 13-7. PNCシートから、ロータリーエンコーダツマミを外します。

3. PNAB Circuit Board Wire Harness

Route this wire harness as far as possible away from harness A (power supply line for the EL panel), then attach tape as shown in the figure below.

3. PNABシート束線

この束線は出来るだけ束線Aより離し、そして下図のようにテープを貼って下さい。



(Fig. 3)

LSI PIN DESCRIPTION (LSI 端子機能表)

• HD6475328CP-10 <H8/532> (XG944B00) CPU (Central Processing Unit)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	XTAL	I	Clock	43	P50/A8	O	Address bus
2	Vss	I	Ground	44	P51/A9	O	
3	P10/ ϕ	O	System clock	45	P52/A10	O	
4	P11/E	O	Enable	46	P53/A11	O	
5	P12/BACK	O	Bus acknowledge	47	P54/A12	O	
6	P13/BREQ	I	Bus request	48	P55/A13	O	
7	P14/WAIT	I	Wait	49	P56/A14	O	
8	P15/IRQ0	I	Interrupt request 0	50	P57/A15	O	
9	P16/IRQ1	I	Interrupt request 1	51	P60/A16	O	
10	P17/TMO	I	8-bit timer output	52	P61/A17	O	
11	P20/AS	O	Address strobe	53	P62/A18	O	
12	P21/R/W	O	Read/Write	54	P63/A19	O	
13	P22/DS	O	Data strobe	55	Vcc	Power supply	
14	P23/RD	O	Read control	56	P70/TMCI	I	8-bit timer clock input
15	P24/WR	O	Write control	57	P71/FT11	I	Free running timer input capture (8-bit timer counter reset input)
16	Vcc		Power supply	58	P72/FT12	I	
17	MDO	I	Mode control	59	P73/FT13/TMRI	I	
18	MD1	I					
19	MD2	I	Standby	60	P74/FT081/FTCI1	O/I	Free running timer output compare B/
20	STBY	I		Reset	61	P75/FT082/FTCI2	O/I
21	RES	I	Non-maskable interrupt		62	P76/FT083/FTCI3	O/I
22	NMI	I		Free running timer output compare A1			
23	NC		63		P77/FTOA1	O	Ground
24	Vss		Ground	64	Vss	Ground	
25	P30/D0	I/O	Data bus	65	AVss	Analog ground	
26	P31/D1	I/O					
27	P32/D2	I/O					
28	P33/D3	I/O					
29	P34/D4	I/O					
30	P35/D5	I/O					
31	P36/D6	I/O					
32	P37/D7	I/O					
33	P40/A0	O		Address bus			
34	P41/A1	O					
35	P42/A2	O					
36	P43/A3	O					
37	P44/A4	O					
38	P45/A5	O					
39	P46/A6	O					
40	P47/A7	O					
41	Vss		Ground				
42	Vss						
				66	P80/ANO	I	Port 8
				67	P81/AN1	I	
				68	P82/AN2	I	
				69	P83/AN3	I	
				70	P84/AN4	I	
				71	P85/AN5	I	
				72	P86/AN6	I	
				73	P87/AN7	I	
				74	AVcc	Analog power supply	
				75	P90/FTOA2	O	Free running timer output compare A2
				76	P91/FTOA3	O	Free running timer output compare A3
				77	P92/PW1	O	Pulse width
				78	P93/PW2	O	
				79	P94/PW3	O	
				80	P95/TXD	O	Transmit data
				81	P96/RXD	I	Receive data
				82	P97/SCK	I/O	Serial clock
				83	Vss	Ground	
				84	EXTAL	I	Clock

• HD63C01Y0F64 (XF148A00) CPU (SEQ.)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	Vss	I	Ground	33	Vcc		DC Supply (+5V)
2	XTAL	I	Clock (8MHz)	34	A15	O	Address bus
3	EXTAL	I					
4	MP0	I	Mode program	35	A14	O	
5	MP1	I					
6	RES	I	Reset	36	A13	O	
7	STBY	I	Stand-by mode signal	37	A12	O	
8	NMI	I	Non-maskable interrupt	38	P11	O	
9	P20/TIN	I/O	Port 2	39	P10	O	
10	P21/TOU1	I/O					
11	P22/SCLK	I/O					
12	P23/RX	I/O					
13	P24/TX	I/O					
14	P25/TOU2	I/O					
15	P26/TOU3	I/O					
16	P27/TCLK	I/O					
17	P50/IRQ1	I/O		Port 5			
18	P51/IRQ2	I/O					
19	P52/MR	I/O					
20	P53/HA1T	I/O					
21	P54/IS	I/O					
22	P55/OS	I/O					
23	P56	I/O					
24	P57	I/O					
25	P60	I/O					
26	P61	I/O					
27	P62	I/O	Port 6				
28	P63	I/O					
29	P64	I/O					
30	P65	I/O					
31	P66	I/O					
32	P67	I/O					
				41	A8	O	
				42	Vss	Ground	
				43	A7	O	
				44	A6	O	
				45	A5	O	
				46	A4	O	
				47	A3	O	
				48	A2	O	
				49	A1	O	
				50	A0	O	
				51	D7	I/O	
				52	D6	I/O	
				53	D5	I/O	
				54	D4	I/O	
				55	D3	I/O	
				56	D2	I/O	
				57	D1	I/O	
				58	D0	I/O	
				59	BA	O	Bus available
				60	LIR	O	Load instruction resistor
				61	R/W	O	Read/Write control
				62	WR	O	Write
				63	RD	O	Read
				64	E	O	Enable

• **YM3413 (XE449A00) LDSP (Digital Signal Processor)**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION	
1	VDD		DC supply (+5V)	21	A5	O	Address bus	
2	D7	I/O		22	A6	O		
3	D6	I/O	Data bus	23	A7	O		
4	D5	I/O		24	A8	O		
5	D4	I/O		25	A9	O		
6	D3	I/O		26	A10	O		
7	D2	I/O		27	A11	O		
8	D1	I/O		28	A12	O		
9	D0	I/O		29	A13	O		
10	SI0	I	Serial data input	30	A14	O		
11	SI1	I		31	A15	O		
12	SYW	I	Sync pulse	32	A16	O		
13	WE	O	Write enable	33	SO0	O		Serial data output
14	OE	O	Output enable	34	XCLK	I		
15	A0	O	Address bus	35	IC	I		Initial Clear
16	A1	O		36	CRS	I		CD counter reset
17	A2	O		37	CDI	I	CD input	
18	A3	O		38	CD _o	O	CD output	
19	A4	O	Ground	39	SO1	O	Serial data output	
20	V _{ss}			40	CLK	I	Clock	

• **YM3415 (XE450A00) LEF (Effect Processor)**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION	
1	V _{DD}		Power supply	21	A7	O	Address bus	
2	SI0	I	Serial data input	22	A6	O		
3	SI1/TST1	I		23	A5	O		
4	SO0	O	Serial data input	24	A4	O		
5	SO1	O		25	A3	O		
6	XCLK	I	Clock	26	A2	O		
7	CDO	O	CD data output	27	A1	O		
8	CDI	I	CD data input	28	A0	O		
9	CRS/CE	I	CD counter reset	29	RAS	O		DRAM control
10	WR	I	Write control	30	CAS	O		DRAM control
11	A/D	I	Address/data parameter select	31	WE	O		WE signal
12	PD0	I/O	Data bus	32	OE	O		OE signal
13	PD1	I/O		33	D3	I/O		
14	PD2	I/O		34	D2	I/O		
15	PD3	I/O		35	D1	I/O		
16	PD4	I/O		36	D0	I/O		
17	PD5	I/O		37	TST2	I	Internal test	
18	PD6	I/O		38	SYW	I	Sync pulse	
19	PD7	I/O		39	CLK	I	Clock	
20	V _{ss}		Ground	40	IC	I	Initial clear	

• **YM3029 (XF237A00) AFD0 (Floating Point Converter)**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	DVDD		Digital power supply (+5V)	15	SHA	I	Sample and hold input (Channel A)
2	LE	O	Latch enable	16	EXG		Exponent ground
3	DAB	O	Channel A/B data output	17	EXG		
4	SYW	I	Sync pulse	18	EXI	I	Exponent input
5	CLK	I	Clock	19	EXO	O	Exponent output
6	φ1	O	Clock for DAC	20	AVSS		Analog power supply (-5V)
7	DGND		Digital ground	21	AVDD		Analog power supply (+5V)
8	ADV _V		Analog power supply (+5V)	22	SI1	I	Serial data input 1 (Channel A)
9	AVSS		Analog power supply (-5V)	23	VLA0	I	Volume level select (Channel A)
10	SHB	I	Sample and hold input (Channel B)	24	VLA1	I	
11	CH4	O	Output (Channel 4)	25	SI2	I	Serial data input 2 (Channel B)
12	CH3	O	Output (Channel 3)	26	VLB0	I	Volume level select (Channel B)
13	CH2	O	Output (Channel 2)	27	VLB1	I	
14	CH1	O	Output (Channel 1)	28	4/2	I	Channel number select (4 or 2-channel)

• YM7102 (XG996A00) PAN (Panning Processor)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION	
1	A0	I	Address bus	41	L8/ACC8	O	L channel data	
2	D7	I/O		42	L9/ACC9	O		
3	D6	I/O		43	L10/ACC10	O		
4	D5	I/O		44	L11/ACC11	O		
5	D4	I/O		45	L12/ACC12	O		
6	D3	I/O		46	L13/ACC13	O		
7	D2	I/O		47	L14/ACC14	O		
8	D1	I/O		48	L15/ACC15	O		
9	D0	I/O		49	R0/ACC16	O		
10	IN1	I	Data from OPS	50	R1/ACC17	O	R channel data	
11	INO	I		51	R2/ACC18	O		
12	SI2	I		52	R3/ACC19	O		
13	SI1	I	Data from PAN (cathcade input)	53	R4	O		
14	TEGSS	I		54	R5	O		
15	TEGS2	I		55	R6	O		
16	TEGS1	I		56	R7	O		
17	TEGS0	I	Test pin	57	R8	O		
18	NC	I		58	R9	O		
19	CDO	O		59	R10	O		
20	CRS	O	Control data for DSP Sync pulse for CD	60	R11	O	R channel data	
21	S1	O		61	R12	O		
22	S2	O	Signal to DSP	62	R13	O		
23	SYW	O		63	R14	O		
24	DSPCLK	O	Sync pulse for DSP	64	R15	O		
25	MODE	I	Clock for DSP	65	NC	I		
			Output mode (L:16bits DAC H:20bits DAC)	66	TTIM	I		
26	IC	I	Initial clear	67	TEG1	I		Test pin
27	SYNC	I	Sync pulse	68	TEG0	I		
28	ϕ_M	I	Clock	69	TRD	I		
29	Vss	I	Ground	70	CS2	I	Chip select	
30	Vdd	I		71	CS1	I		
31	Vdd	I		Power supply	72	Vdd		I
32	Vdd	I	73		CS0	I		
33	L0/ACCO	O	74		A7	I		
34	L1/ACC1	O	L channel data	75	A6	I	Address bus	
35	L2/ACC2	O		76	A5	I		
36	L3/ACC3	O		77	A4	I		
37	L4/ACC4	O		78	A3	I		
38	L5/ACC5	O		79	A2	I		
39	L6/ACC6	O		80	A1	I		
40	L7/ACC7	O						

• μ PD71055C (XB361001) PPI (Programmable Peripheral Interface)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	PO3	I/O	Port 0	21	P13	I/O	Port 2
2	PO2	I/O		22	P14	I/O	
3	PO1	I/O		23	P15	I/O	
4	PO0	I/O		24	P16	I/O	
5	RD	I	Read control Chip Select	25	P17	I/O	DC Supply
6	CS	I		26	V _{DD}	I	
7	GND	I	DC Supply (0V)	27	D7	I/O	
8	A1	I	Port address	28	D6	I/O	Data bus
9	A2	I		29	D5	I/O	
10	P27	I/O	Port 2	30	D4	I/O	
11	P26	I/O		31	D3	I/O	
12	P25	I/O		32	D2	I/O	
13	P24	I/O		33	D1	I/O	
14	P20	I/O		34	D0	I/O	
15	P21	I/O		35	RESET	I	Reset Write control
16	P22	I/O		36	WR	I	
17	P23	I/O	Port B	37	P07	I/O	Port 0
18	P10	I/O		38	P06	I/O	
19	P11	I/O		39	P05	I/O	
20	P12	I/O		40	P04	I/O	

• **YM7103 (XG993A00) EGM2 (Envelope Generator)**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	A0	I	Address bus	41	NC		Key on data
2	D7	I/O		42	KON	O	
3	D6	I/O		43	E0	O	
4	D5	I/O		44	E1	O	
5	D4	I/O		45	E2	O	
6	D3	I/O		46	E3	O	
7	D2	I/O		47	E4	O	
8	D1	I/O		48	E5	O	
9	D0	I/O		49	E6	O	
10	NC		50	E7	O	Envelope data, Pitch data (portament), Pitch envelope data	
11	TST10	O	51	E8	O		
12	TST9	O	52	E9	O		
13	TST8	O	53	E10	O		
14	TST7	O	54	E11	O		
15	TST6	O	55	E12	O		
16	TST5	O	56	E13	O		
17	TST4	O	57	NC			
18	TST3	O	58	NC			
19	TST2	O	59	NC			
20	TST1	O	60	NC			
21	TST0	O	61	NC			
22	ϕ M0	O	62	NC			
23	XTAL	O	Quartz crystal	63	NC		
24	EXTAL	I		64	NC		
25	IC	I	Initial clear	65	NC		
26	SY0	O	Sync pulse	66	NC		
27	SY1	I	Sync pulse	67	NC		
28	ϕ M1	I	Clock	68	NC		
29	Vss		Ground	69	NC		
30	Vss			70	NC		
31	NC		Power supply	71	TRD	I	Test pin
32	V _{DD}			72	V _{DD}		Power supply
33	NC			73	CS0	I	Chip select
34	NC		74	CS1	I		
35	NC		75	CS2	I		
36	TEGS2	I	Test pin	76	A5	I	Address bus
37	TEGS1	I		77	A4	I	
38	TEGSO	I		78	A3	I	
39	TSO1	O		79	A2	I	
40	TSO0	O	80	A1	I		

• **WD37C65B-JM00 (XH129A00) FDC (Floppy Disk Controller)**

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	RD	I	Read control	23	XT2	I	XTAL osc. in
2	WR	I	Write control	24	DRV	I	Drive type
3	CS	I	Chip select	25	XT1	O	XTAL osc. drive
4	AO	I	Register select	26	XT1	I	XTAL osc. in
5	DACK	I	DMA acknowledge	27	PCVAL	I	Precompensation value
6	TC	I	Terminal Count	28	HS	O	Head select (Side select)
7	DB0	I/O	Data bus	29	WE	O	Write enable
8	DB1	I/O		30	WD	O	Write data
9	DB2	I/O		31	DIRC	O	Direction control
10	DB3	I/O		32	STEP	O	Step pulse
11	DB4	I/O		33	DS1	O	Drive select 1
12	DB5	I/O		34	V _{SS}		Ground
13	DB6	I/O		35	DS2	O	Drive select 2
14	DB7	I/O	36	M01/DS3	O	Motor ON 1/Drive select 3	
15	DMA	O	Direct memory access request	37	M02/DS4	O	Motor ON 2/Drive select 4
16	IRQ	O	Interrupt request	38	HDL	O	Head loaded
17	DCHGEN	O	Disk change enable	39	RPM/RWC	O	Revolutions per minute/Reduced write current
18	LDOR	I	Load operations register	40	DCHG	I	Disk change
19	LDCR	I	Load control register	41	WP	I	Write protected
20	RST	I	Reset	42	TR00	I	Track 00 signal
21	RDD	I	Read disk data	43	IDX	I	Index
22	XT2	O	XTAL osc. drive	44	V _{CC}		Power supply

• YM7107 (XG994A00) OPS3 (Operator)

PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION	
1	A0	I	Address bus	41	DA8	O	D/A signal (straight binary) (MSB)	
2	D7	I/O		42	DA9	O		
3	D6	I/O	Data bus	43	DA10	O		
4	D5	I/O		44	DA11	O		
5	D4	I/O		45	DA12	O		
6	D3	I/O		46	DA13	O		
7	D2	I/O		47	DA14	O		
8	D1	I/O		48	DA15	O		
9	D0	I/O		49	SH1	O		
10	E13	I		50	SH2	O		
11	E12	I	Channel distribution	51	SC0	O		
12	E11	I		52	SC1	O		
13	E10	I		53	SC2	O		
14	E9	I	Envelope data, Pitch envelope data, Pitch data	54	SO0	O		Serial data (2 compl. 16bits LSB first)
15	E8	I		55	SO1	O		
16	E7	I		56	NC			
17	E6	I		57	NC			
18	E5	I		58	NC			
19	E4	I		59	NC			
20	E3	I		60	NC			
21	E2	I		61	NC			
22	E1	I		62	NC			
23	E0	I		63	NC			
24	KON	I	Phase reset for phase accumulator Initial clear	64	NC			
25	IC	I		65	NC			
26	NC		66	NC				
27	SYNC	I	Sync pulse (127C127)	67	NC			
28	ϕ_M	I	Clock	68	Vss			
29	Vss		Ground	69	S10	I	Serial data	
30	Vss			70	S11	I		
31	VDD		Power supply	71	NC			
32	VDD			72	VDD			
33	DA0	O	(LSB)	73	CS0	I	Chip select	
34	DA1	O		74	CS1	I		
35	DA2	O		75	CS2	I		
36	DA3	O	D/A signal (straight binary)	76	A4	I	Address bus	
37	DA4	O			77	A3		I
38	DA5	O			78	A2		I
39	DA6	O			79	A1		I
40	DA7	O		80	Vss		Ground	

• HD637B01Y (XG950A00) CPU (PKS)

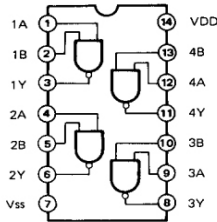
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION	
1	Vss		Ground	33	Vcc		DC Supply (+5V)	
2	XTAL	I	Clock (8MHz)	34	P47	O	Port 4	
3	EXTAL	I			35	P46		O
4	MP0	I	Mode program	36	P45	O		
5	MP1	I			37	P44		O
6	RES	I	Reset	38	P43	O		
7	STBY	I	Stand-by mode signal	39	P42	O		
8	NMI	I	Non-maskable interrupt	40	P41	O		
9	P20	I/O	Port 2	41	P40	O		
10	P21	I/O			42	Vss		
11	P22	I/O			43	P17	O	Ground
12	P23	I/O			44	P16	O	
13	P24	I/O			45	P15	O	Port 1
14	P25	I/O			46	P14	O	
15	P26	I/O		47	P13	O		
16	P27	I/O	Port 5	48	P12	O	Port 3	
17	P50	I/O			49	P11		O
18	P51	I/O			50	P10		O
19	P52	I/O			51	P37		I/O
20	P53	I/O			52	P36		I/O
21	P54	I/O			53	P35		I/O
22	P55	I/O	Port 6	54	P34	I/O	Port 7	
23	P56	I/O			55	P33		I/O
24	P57	I/O			56	P32		I/O
25	P60	I/O			57	P31		I/O
26	P61	I/O			58	P30		I/O
27	P62	I/O			59	P74		O
28	P63	I/O	Port 6	60	P73	O	Port 7	
29	P64	I/O			61	P72		O
30	P65	I/O			62	P71		O
31	P66	I/O			63	P70		O
32	P67	I/O		64	E	O	Enable	

• YM7119 (XG995A00) M3 (AWM Tone generator & Digital Filter)

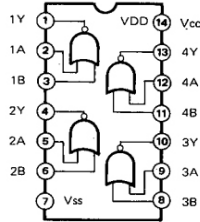
PIN NO.	NAME	I/O	FUNCTION	PIN NO.	NAME	I/O	FUNCTION
1	INDV0	O	Individual output 0 (8 channels)	65	WA8	O	Wave memory address bus
2	INDV1	O	Individual output 1 (8 channels)	66	WA9	O	
3	OPZ	I	MELIN input select (⊕ OPZ, ⊖ PÂN)	67	WA10	O	
4	DIOU0	O	Stereo output (L & R)	68	WA11	O	
5	DIOU1	O	Assignable output (ch.0 & ch.4)	69	WA12	O	
6	DIOU2	O	Assignable output (ch.1 & ch.5)	70	WA13	O	
7	DIOU3	O	Assignable output (ch.2 & ch.6)	71	WA14	O	
8	DIOU4	O	Assignable output (ch.3 & ch.7)	72	NC		
9	MELIN	I	MEL formatted signal input	73	WA15	O	
10	LSB/MSB	I	Individual output mode select	74	WA16	O	
11	TTPAD0	I/O	(⊕ MSB first, ⊖ LSB first)	75	WA17	O	
12	TTPAD1	I/O		76	WA18	O	
13	NC			77	WA19	O	
14	TTPAD2	I/O		78	WA20	O	
15	TTPAD3	I/O		79	WA21	O	
16	TTPAD4	I/O		80	WA22	O	
17	TTPAD5	I/O		81	WA23	O	
18	NC			82	A0	I	
19	TTPAD6	I/O	Test pin	83	A1	I	
20	TTPAD7	I/O		84	A2	I	
21	NC			85	A3	I	
22	TTPAD8	I/O		86	A4	I	
23	TTPAD9	I/O		87	A5	I	
24	NC			88	D0	I/O	
25	TTPAD10	I/O		89	NC		
26	TTPAD11	I/O		90	D1	I/O	
27	DIINO	I	Individual input 0 (8 channels)	91	D2	I/O	
28	DIIN1	I	Individual input 1 (8 channels)	92	D3	I/O	
29	WDO	I/O		93	D4	I/O	
30	WD1	I/O		94	D5	I/O	
31	WD2	I/O		95	D6	I/O	
32	WD3	I/O		96	D7	I/O	
33	NC			97	S/HSC0	I	
34	WD4	I/O		98	S/HSC1	I	
35	WD5	I/O		99	S/HSC2	I	
36	WD6	I/O		100	S/HSC3	I	
37	WD7	I/O	Wave memory data	101	S/HEN	O	
38	WD8	I/O		102	S/H0	O	
39	WD9	I/O		103	S/H1	O	
40	NC			104	S/H2	O	
41	NC			105	S/HRCA	I	
42	WD10	I/O		106	S/HRCB	I	
43	WD11	I/O		107	IC	I	
44	NC			108	Vss	Ground	
45	WD12	I/O		109	XTAL	O	
46	WD13	I/O		110	EXTAL	I	
47	WD14	I/O		111	NC		
48	Vss		Ground	112	FCLKOUT	O	
49	Vdd		Power supply	113	FCLKIN	I	
50	WD15	I/O		114	NC		
51	MSBW	O	Wave data MSB write signal	115	CLK3	O	
52	LSBW	O	Wave data LSB write signal	116	VDD	Power supply	
53	OE	O	Output enable for wave data	117	SYWIN	I	
54	ODD/EVEN	I	Odd/Even select on 2 chips mode	118	CLKMEL	O	
55	SINGLE/DUAL	I	Wave memory single/dual mode select (⊕: dual-2 chips mode, ⊖: single-1 chip mode)	119	NC		
56	WA0	O		120	DACLE	O	
57	WA1	O		121	SYWOUT	O	
58	WA2	O		122	SYW64	O	
59	WA3	O		123	IRQ	O	
60	WA4	O		124	CS	I	
61	WA5	O	Wave memory address bus	125	R/W	I	
62	WA6	O		126	CHPIN	I	
63	WA7	O		127	CHPOUT	O	
64	NC			128	KSYNC	I	

■ IC BLOCK DIAGRAM (ICブロック図)

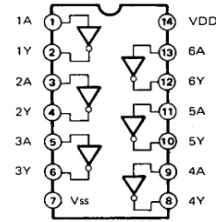
- 74F00PC (IG063690)
Quad 2 Input NAND



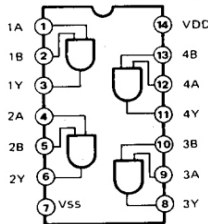
- SN74HC02N (IR000250)
Quad 2 Input NOR



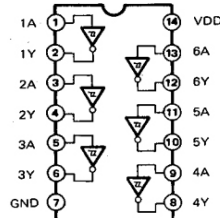
- SN74LS04N (IG027020)
- SN74HCU04N (IG142250)
- SN74HC04NSR (XD830A00)
- HD74LS05P (IG052600)
Hex Inverter



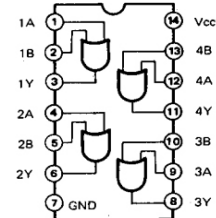
- SN74ALS08N (XA876001)
Quad 2 Input AND



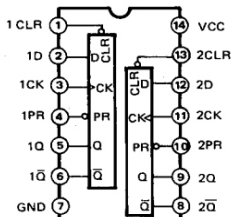
- SN74HC14N (IR001450)
Hex Inverter



- 74F32PC (IG058990)
- SN74HC32N (IR003250)
- SN74ALS32N (XA055001)
- SN74LS32N (IG049850)
Quad 2 Input OR

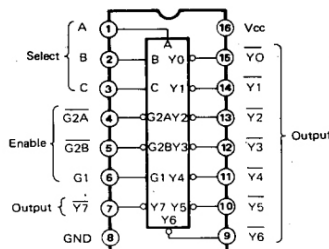


- SN74HC74N (IR007450)
- SN74ALS74N (XA196A00)
Dual D-Type Flip-Flop

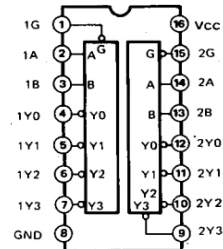


INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q _o	Q̄ _o

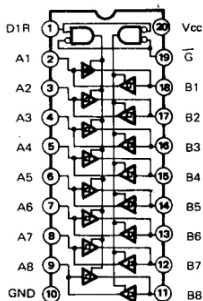
- 74F138PC (IG120090)
- SN74ALS138N (IG149600)
- SN74HC138N (IR013850)
3 to 8 Demultiplexer



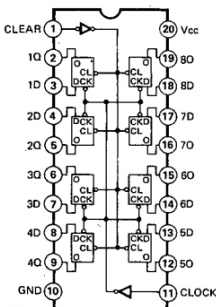
- SN74HC139N (IR013950)
Dual 2 to 4 Demultiplexer



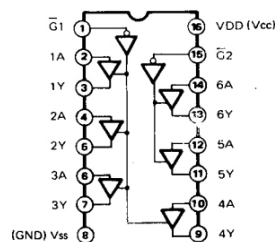
- **SN74ALS245AN** (IG149900)
- **TC74HC245P** (IR024500)
- **SN74LS245** (IG044600)
Octal 3-State Bus Transceiver



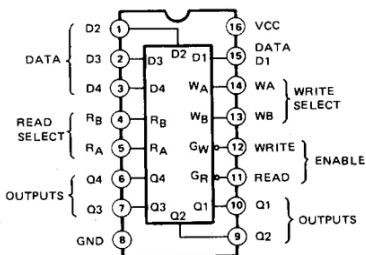
- **SN74HC273N** (IR027350)
Octal D-Type Flip-Flop



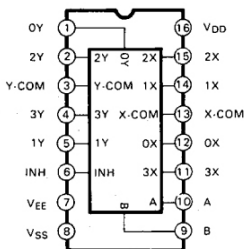
- **SN74HC367N** (IR036750)
Hex 3-State Bus Buffer



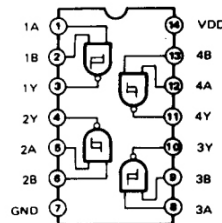
- **HD74LS670P** (IG115300)
4-4 Register Files (3-States)



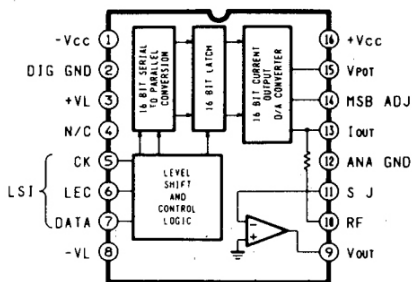
- **TC74HC4052AP** (IR405200)
Differential 4-Channel Multiplexer/Demultiplexer



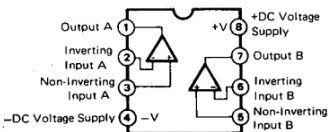
- **TC4093BP** (IG043300)
Quad 2-Input NAND Schmitt Trigger



- **PCM56P** (XB637001)
Digital Analog Converter



- **M5238P** (XA013001)
- **RC4558D-V** (IG001390)
- **NJM4556** (IG042500)
Dual Operational Amplifier



SY77

■ ERROR MESSAGES

MIDI	
Display	Error Message
MIDI buffer full !	When the SY77 attempted to receive or transmit a large amount of MIDI data, its handling capacity was exceeded.
MIDI data error !	An error occurred when receiving MIDI data.
MIDI checksum err !	An error occurred when receiving bulk data.
Data empty !	There is no data to transmit.
Bulk rejected; song exist !	Since the selected song number already exists in sequencer memory, the sequence data (bulk) was not received. Select an unused song.
Song memory full !	When receiving sequence data (bulk), the internal memory capacity was exceeded, and not all the data was received.
Device number is off !	Since the device number is off, bulk data cannot be transmitted or received.
Device number mismatch !	Since the device numbers did not match, the bulk data was not received.
Bulk canceled by EXIT !	While receiving bulk data, EXIT was pressed to abort the operation.
Bulk protected !	Since the bulk protect is on, the bulk data was not received.

Data card	
Display	Error Message
Data card not ready !	The data card is not correctly inserted into the slot.
Card protected !	Since the memory protect switch of the card is on, data cannot be saved to the card.
Illegal format !	The card is the wrong format.
Verify error !	The data was not correctly saved.

Wave card	
Display	Error Message
Wave card not ready !	The wave card is not correctly inserted into the slot.
Different wave card (ID =) !	The wave card which is inserted is not the one used by the voice or multi.
ID Number mismatch !	A multi includes voices which use two or more wave.

Disk	
Display	Error Message
Disk not ready !	The disk is not correctly inserted into the disk drive.
Illegal change !	During the backup operation, the original and back up disks were inserted in the wrong order.
Illegal disk !	The data in the disk is faulty.
Bad disk !	The disk is faulty.
File not found !	The file was not found.
Write protected !	The disk is write protected.
Disk full !	There is no more memory available on the disk.
Directory full !	The directory area on the disk is full, and new files cannot be created.
Media type error !	The disk is the wrong type.
Illegal file !	The file is not for the SY77.
Sequencer memory full !	The sequencer memory is full.

Sequencer and display	
Display	Error Message
Please stop sequencer !	The sequencer cannot play during disk or card loading or saving or during bulk data transmission.
Illegal time !	You attempted to execute the Get Pattern operation, but the time signature was incorrect.
Range is exceeded !	The parameter you specified in an edit job is beyond the valid range.
Data not Found !	When you executed the Search Part operation in Chain Pattern, the specified data was not found.
Illegal input !	You attempted to enter an invalid data value in Edit Insert mode.
Internal buffer full !	More sequence data was played back than could be sounded.

Battery	
Display	Error Message
Change internal battery !	The internal backup battery needs to be replaced.
Change card battery !	The card backup battery needs to be replaced.

Other	
Display	Error Message
Use bank D !	4 element voices can be stored (or copied) only to bank D.
Please stop sequencer !	Please stop the sequencer and try the operation once again.
Illegal mark !	You attempted to mark a display which does not allow marking.
Use bank A-C !	The voice must be stored in bank A, B, or C.

■ エラーメッセージ

MIDI関係	
ディスプレイ表示	メッセージの内容
MIDI buffer full !	一度に多量のMIDIデータが送受信されたため、送受信ができません。データ量を減らしてください。
MIDI data error !	MIDIデータを受信した際、異常がありました。
MIDI checksum err !	バルクデータの受信の際、異常がありました。
Data empty !	シーケンスデータ(バルク)を送信しようとしたのですが、データが内部にありません。
Bulk rejected; song exists !	現在選ばれているソング番号に、すでに別のデータが入っているため、シーケンスデータ(バルク)を受信できません。
Bulk canceled by EXIT !	シーケンスバルクデータ受信中にEXITが押されたので、データの受信を中止しました。シーケンスデータはクリアされた状態となります。
Song memory full !	シーケンスデータ(バルク)を受信した際、内部メモリーが一杯になってしまい、データを全て受信できません。
Bulk protected !	バルクプロテクトがオンになっているため、バルクデータの受信ができません。
Device number is off !	デバイスナンバーがオフになっているため、バルクデータの送受信ができません。
Device number mismatch !	デバイスナンバーのチャンネルが一致していないため、バルクデータの受信ができません。

データカード関係	
ディスプレイ表示	メッセージの内容
Data Card not ready !	カードが本体に正しくセットされていません。
Card protected !	カード自体のプロテクトスイッチがオンになっているため、データのセーブおよびオートストアができません。
Illegal format !	カードのフォーマットが違います。
Verify error !	カードのセーブが正しく行われていません。

ウェイブカード関係	
ディスプレイ表示	メッセージの内容
Wave card not ready !	ウェイブカードが本体に正しくセットされていません。
Different wave card (ID=) !	プレイしようとしているボイスで使用されるべきウェイブフォームは、現在カードスロットにセットされているものと異なるウェイブフォームカードのものです。
ID Number mismatch !	同時には、1つのウェイブフォームカードしか使用できないにも関わらず、マルチを構成する各々のボイスが必要とするウェイブフォームカードが異なるため、正常に発音しません。

ディスク関係	
ディスプレイ表示	メッセージの内容
Disk not ready !	ディスクが本体に正しくセットされていません。
Illegal change !	バックアップ作業中に、新旧のディスクの順番を間違えて挿入しました。
Illegal disk !	ディスク内のデータ不良です。
Bad disk !	ディスク不良です。
File not found !	ファイルが見つかりません。
Write protected !	ディスクがプロテクトされています。
Disk full !	ディスクのメモリーが一杯です。
Directory full !	ディレクトリのエリアが一杯で、ファイルが作れません。
Media type error !	ディスクの種類が違います。
Illegal file !	本機用のファイルではありません。
Sequencer memory full !	シーケンス用の内部メモリーが一杯です。

シーケンサー関係	
ディスプレイ表示	メッセージの内容
Please stop sequencer !	ディスク、カードとのロード、セーブあるいは、バルクトランスミットなどは、シーケンサーがプレイされているときに実行することはできません。
Illegal time !	ゲットパターンを実行しようとしたが、設定されている拍子が異なっています。
Range is exceeded !	エディットジョブで指定したパラメータは設定できる範囲を超えています。
Data not Found !	チェインパターンでサーチパートを実行したが、目的のデータはありませんでした。
Illegal input !	エディットのインサートモードで入力しようとしたデータの値が正しくありません。
Internal buffer full !	シーケンサーを再生している時、シーケンスデータが多くて全てを発音することができません。

電池関係	
ディスプレイ表示	メッセージの内容
Change internal battery !	本体内のバックアップバッテリーが寿命です。
Change card battery !	カードのバックアップバッテリーが寿命です。

その他	
ディスプレイ表示	メッセージの内容
Use bank D !	4エレメントタイプのボイスは、バンクDにしかストアできません。 Disk 1 Voice loadの時、セーブ時にバンクDにあったボイスは、バンクDにしかロードできません。
Use bank A-C !	Disk 1 Voice loadの時、セーブ時にバンクA-Cにあったボイスは、バンクA-Cにしかロードできません。
Illegal mark !	現在の画面には、マークすることはできません。

■ TEST PROGRAM

VERSION DISPLAY MODE

In order to verify the ROM versions of the SY77, you may want to initiate the Version Display Mode. To initiate this mode press and hold the [Voice], the [INTERNAL], and the [1] switches then the versions of the MAIN ROM and SEQUENCE (SEQ) ROM will be displayed. Press [EXIT] to return to the main program.

A. HOW TO ENTER THE TEST PROGRAM

Turn on the power switch of the SY77 and wait until the LCD has initialized and displays a normal operating mode message. While pressing the [VOICE] switch, press and hold the [BANK D] switch then the [8] switch. The SY77 will run the INITIAL TEST routine (refer to the INITIAL TEST section for details) and indicate that you have entered the Test Program by displaying the following message.

```

*** SY77 TEST Ver #.## *** Please Select

Main ROM : Version #.#   1989-10-??
SEQ. ROM : Version #.#   1989-10-??

[-1] : AUTO           [+1] : MANUAL

[ COPY ] : Fact.set   [EXIT] : Exit
  
```

Use the [-1], [+1], [COPY], or [EXIT] panel switches to select the appropriate test mode. If you press [-1], the auto test mode will be initiated. If you press [+1], the MANUAL test mode will be initiated. If you press [COPY], the SY77 will execute Test 48, "48. Factory settings", and then automatically exit the test mode and return to play mode (refer to Test 48 for details).

If you press [EXIT], you will exit the test mode and return to the play mode. The MANUAL mode is the preferred method of running the test program because it allows you to select or jump to any test and execute it. AUTO mode automatically executes each test in a fixed order. Some of the tests in the AUTO mode are automatically executed due to the nature of the test. In the AUTO mode simply press the [+1] switch to exit and automatically execute the next test or press [EXIT] to abort the test, then press [+1] to automatically execute the next test.

B. PROCEEDING THROUGH THE TESTS

(**MOST OF THESE FUNCTIONS MAINLY PERTAIN TO THE MANUAL TEST MODE**)

When you enter the test program, the following display will appear.

```

*** SY77 TEST Ver #.## *** MODE : MANUAL

* 01 : ROM CHECK
  02 : RAM Read/Write
  03 : SEQUENCER ROM
  04 : SEQUENCER RAM
  05 : RAM Battery
  
```

Use the [+1], [-1], [ENTER], [COPY], [PAGE+], [PAGE-], [EXIT], or the numeric key pad, or the rotary encoder to move through the various tests of the test program.

Pressing: [+1] will execute the test which follows the current test.

[-1] will execute the test which precedes the current test.

[ENTER] will execute the currently selected test.

[PAGE+] will select the test which follows the current test and displays the test items.

[PAGE-] will select the test which precedes the current test and displays the test items.

[EXIT] will execute Test 49, "49. EXIT" (refer to Test 49 for details).

The numeric keys 0 through 9 of the entry pad can be used to enter a two-digit number to directly select a test. Simply enter the number and then press the [ENTER] switch. For example, if you would like to select TEST 6, press [0], [6] then press the [ENTER] switch.

TEST SELECTION WHEN AN ERROR IS DETECTED

In each of the following tests listed below, if an NG (No Good) error is detected, the following operations of the test will make the SY77 wait for the entry of a test number. You can then retry the test or perform another test. If you press [EXIT], the SY77 will wait for the entry of a test number.

- | | | |
|------------------------|-------------------------|------------------------|
| 9. Panel switches | 10. Pitch bend | 11. Modulation wheel 1 |
| 12. Modulation wheel 2 | 13. Data entry | 14. Rotary encoder |
| 15. Keyboard | 16. Aftertouch | 17. MIDI IN/OUT/THRU |
| 18. Card insert | 20. Card protect switch | 22. Wave card insert |
| 25. Disk eject | 26. Breath controller | 27. Foot volume |
| 28. Foot controller | 29. Sustain switch | 30. Foot switch |
| 47. Jacks all off | | |

INITIAL TEST

The following tests will be performed automatically when the test program is initiated.

- A. Read/write check for the SRAM (IC130) work area of the DM1 circuit board.
- B. Checks the interrupt levels of both M3 ICs (IC205 & IC228) of the DM2 circuit board.

DISPLAY OF TEST RESULTS

If each test checks OK then the Test program proceeds to the Test Program entry display. If Test A is NG the RAM WORK AREA may be at fault and the display will indicate:

```
** IC130(RAM) ERROR, TEST ABOARTED **
```

If Test B is NG then the error may be related to one of the M3 IC's IRQ levels. The display will indicate the error by showing the following message:

```
* M3 IRQ CHECK ERROR, TEST ABOARTED *
```

EXITING THE TEST

This test automatically proceeds to the Test Program entry display if the items under test are OK. If an error message occurs turn the power off and then on again to exit the test. However, a RAM ERROR may not allow the SY77 to function normally.

TEST PROGRAM TEST 1-49 (MANUAL MODE OPERATION)**1. TEST 1: SYSTEM ROM TEST**

```
* 01; ROM CHECK
```

Performs a read test on the ROM for the following addresses.

IC123 : 80000h-8000Fh IC124 : A0000h-A000Fh

IC125 : C0000h-C000Fh IC126 : E0000h-E000Fh

(This test checks only 16 bytes.)

DISPLAY OF TEST RESULTS

```
OK      * 01: ROM CHECK      4:IC126      OK
```

(the number of the last-tested IC)

or

```
NG      * 01: ROM CHECK      n:ICxxx      NG
```

(where n=ROM# and xxx=IC#)

TEST END

Ends after displaying the results.

2. TEST 2: SYSTEM RAM TEST

* 02: RAM Read/Write

Performs a read/write test of RAM on the following addresses.

IC127 : 40000h–47FFFh

IC128 : 48000h–4FFFFh

IC129 : 50000h–57FFFh

IC130 : 58000h–5FFFFh (Only 1024 bytes)

DISPLAY OF TEST RESULTS

OK	* 02: RAM Read/Write	4:IC130	OK
----	----------------------	---------	----

(the number of the last-tested IC)

or

NG	* 02: RAM Read/Write	n:ICxxx	NG
----	----------------------	---------	----

(where n=RAM# and xxx=IC#)

TEST END

Ends after displaying the results. All RAM data is preserved.

3. TEST 3: SEQUENCER ROM TEST

* 03: SEQUENCER ROM

Performs a read test on the ROM (IC151) of DM1 circuit board.

DISPLAY OF TEST RESULTS

OK	* 03: SEQUENCER ROM	OK
----	---------------------	----

NG	* 03: SEQUENCER ROM	NG
----	---------------------	----

TEST END

Ends after displaying the results.

4. TEST 4: SEQUENCER RAM TEST

* 04: SEQUENCER RAM

Performs a RAM read/write test on all addresses of IC153 (RAM 1), IC158 (RAM 2) and IC159 (RAM 3).

DISPLAY OF TEST RESULTS

OK	* 04: SEQUENCER RAM	123	OK
----	---------------------	-----	----

NG	* 04: SEQUENCER RAM	1x3	NG
----	---------------------	-----	----

(e.g. if RAM 2 is NG, an x will mark out the RAM 2 number indicating that it is no good.)

TEST END

Ends after displaying the results. All RAM data is preserved.

5. TEST 5: RAM BACKUP BATTERY TEST

* 05: RAM Battery

This test checks that the voltage of the RAM backup battery is greater than 2.8V and less than 4.1V.

DISPLAY OF TEST RESULTS

OK	* 05: RAM Battery	3.2V	OK
NG	* 05: RAM Battery	#. #V Low	NG
	* 05: RAM Battery	#. #V High	NG

TEST END

Ends after displaying the test results.

6. TEST 6: LCD – ALL DOTS “ON” TEST

* 06: LCD All On

Check that all dots of the LCD change to black (ON).

DISPLAY OF TEST RESULTS

First, the display indicates “* 06 LCD All On”, then all dots of the LCD change to black (ON).

TEST END

Press [EXIT] to end the test. The display shown below will appear and the SY77 will wait for you to enter a test number.

* 06: LCD All On

7. TEST 7: LCD – ALL DOTS “OFF” TEST

* 07: LCD All Off

Check that all dots change to white (OFF).

DISPLAY OF TEST RESULTS

First, the display indicates “* 06 LCD All OFF”, then all dots of the LCD change to white (OFF).

TEST END

Press [EXIT] to end the test. The display shown below will appear and the SY77 will wait for you to enter a test number.

* 07: LCD All Off

8. TEST 8: LED ON/OFF TEST

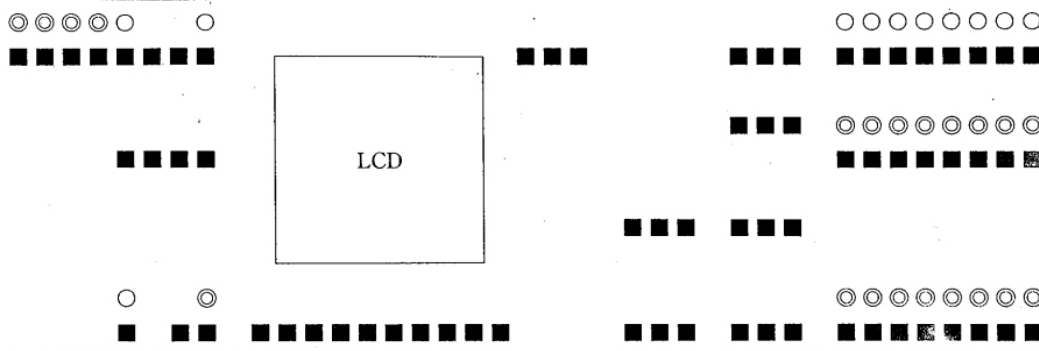
* 08: LED Check

Check that each red LED blinks once in succession from the left end of the unit (refer to the diagram shown below) and then verify that all red LEDs blink together. Next, check that each green LED blinks once, and then all green LEDs blink together. The currently blinking LEDs will be displayed in the LCD as follows.

* 08: LED Check REC RED On

(e.g. The red RECORD LED is blinking)

Check that all LEDs blink. (21 of the 32 LEDs are dual-color red/green LEDs)



Note: (◎) indicates a dual-color LED. (○) indicates a single-color LED.

TEST END

Press [EXIT] to end the test. The SY77 will then be waiting for the entry of a test number.

9. TEST 9: PANEL SWITCH TEST

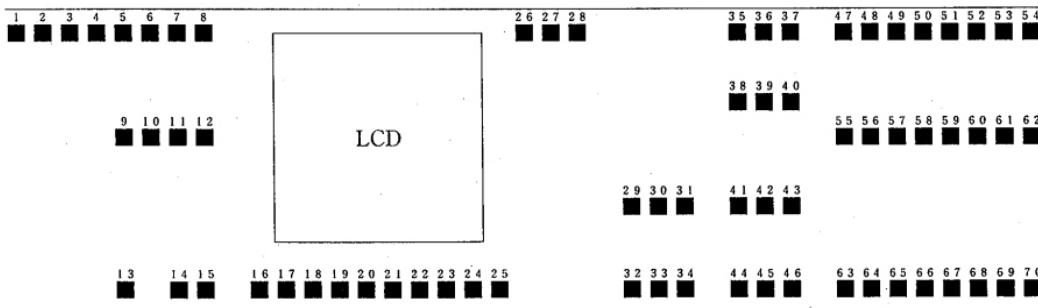
* 09: Panel Switch

Press the panel switches consecutively from the [VOICE] switch to switch [16], according to the order indicated by the LCD display.

* 09: Panel Switch Push REC

(e.g. When checking [RECORD])

The switch pressing order is displayed in the diagram below. If the switch is OK, a beep will sound and you should proceed to test the next switch. If the wrong switch is pressed an unexpected code is sent from the PKS CPU, and the error message NG will be displayed and no sound will be heard. At this time, if the correct switch is pressed then the proper code is received. You will then be able to proceed to test the next switch. The display will indicate OK, if all switches are good.



DISPLAY OF TEST RESULTS

OK * 09: Panel Switch Push 16 OK

NG * 09: Panel Switch Push REC 1? Err

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TEST END

When switch [16] is pressed, OK is displayed and the test will end. During the test, if NG is detected, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

10. TEST 10: PITCH BEND WHEEL TEST

* 10: Pitch Bend	50	99
------------------	----	----

According to the target value displayed on the LCD, slowly move the pitch bend wheel. Check that the value changes from 50 to 99 then to 00 and back to 50 (in other words, center to top then to bottom and back to center).

* 10: Pitch Bend	xx	yy
------------------	----	----

(where xx = current pitch bend value and yy = next target value)

DISPLAY OF TEST RESULTS

OK	* 10: Pitch Bend	50	50	OK
----	------------------	----	----	----

NG	* 10: Pitch Bend	xx	Center	NG
----	------------------	----	--------	----

(If the pitch bend value at the beginning or end of the test is not center, then xx indicates the pitch bend value when NG was detected).

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

11. TEST 11: MODULATION WHEEL 1 TEST

* 11: Modulation W11	00	20-80
----------------------	----	-------

According to the target value displayed on the LCD, slowly move modulation wheel 1. Check that the value changes from 00→20→80→99 then back down to 80→20→00 (in other words, from bottom to top the back to the bottom).

* 11: Modulation W11	xx	yy
----------------------	----	----

* 11: Modulation W11	xx	yy-zz
----------------------	----	-------

(where xx = current value of modulation wheel 1, yy and zz are the next target values)

DISPLAY OF TEST RESULTS

OK	* 11; Modulation W11	00	00	OK
----	----------------------	----	----	----

NG (No change in display message)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

12. TEST 12: MODULATION WHEEL 2 TEST

* 12: Modulation WH2	50	99
----------------------	----	----

Before beginning this test, move modulation wheel 2 to the center position. According to the target value displayed on the LCD, slowly move modulation wheel 2. Check that the value changes from 50 to 99 then to 00 and back to 50 (in other words, from center to top then to bottom and back to center).

* 12: Modulation WH2	xx	yy
----------------------	----	----

* 12: Modulation WH2	xx	yy-zz
----------------------	----	-------

(where xx = current value of modulation wheel 2, yy and zz are the next target values)

DISPLAY OF TEST RESULTS

OK	* 12: Modulation WH2	50	50	OK
----	----------------------	----	----	----

NG (No change in display message)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

13. TEST 13: DATA ENTRY SLIDER TEST

* 13: Data Entry	00	20-80
------------------	----	-------

According to the target value displayed on the LCD, slowly move the data entry slider. Check that the value changes from 00→20→80→99 and the back down to 80→20→00 (in other words, from the bottom to the top and back down to the bottom).

* 13: Data Entry	xx	yy
------------------	----	----

* 13: Data Entry	xx	yy-zz
------------------	----	-------

(where xx = current value of data entry, yy and zz are the next target values)

DISPLAY OF TEST RESULTS

OK	* 13: Data Entry	00	00	OK
----	------------------	----	----	----

NG (No change in display message)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

14. TEST 14: ROTARY ENCODER (DATA ENTRY WHEEL) TEST

* 14: R-Encoder	Right	00
-----------------	-------	----

Rotate the rotary encoder (data entry wheel) to the right as indicated by the LCD display. Check that the value on the LCD changes from Right 00→Left 00→Left 01 (in other words, first rotate to the right then to the left).

* 14: R-Encoder	Right	xx
-----------------	-------	----

* 14: R-Encoder	Left	xx
-----------------	------	----

(where xx = current value)

DISPLAY OF TEST RESULTS

OK	* 14: R-Encoder	Left	01	OK
----	-----------------	------	----	----

NG (No change in display message)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

15. TEST 15: KEYBOARD TEST

* 15: Keyboard Check

Play a scale on the keyboard from C1 to C6 with a steady and even touch.

* 15: Keyboard Check	Push	C1
----------------------	------	----

(e.g. in the case of C1)

If the key switch is ok, the note will sound and you should proceed to play the next key. If you play the wrong key this will produce an unexpected code to the PKS CPU and Err will be displayed. As a result the sound of that note will not be heard. However, if the right key is played following the playing of the wrong key, then correct code is received and the note for that key will sound. You can then proceed to play the next key. If all key switches are good then OK will be displayed on the LCD.

DISPLAY OF TEST RESULTS

OK	* 15: Keyboard Check	Push	C6	OK
----	----------------------	------	----	----

NG	* 15: Keyboard Check	Push	xxx I7 Err
----	----------------------	------	------------

(if play the wrong key)

NG	* 15: Keyboard Check	Push	xxx \$nn NG
----	----------------------	------	-------------

(if the initial touch was incorrect)

TEST END

When you play the C6 key and OK is displayed, the test will end.

If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

16. TEST 16: AFTERTOUCH TEST

```
* 16: After Touch  00  20-80
```

According to the target value displayed on the LCD, press a key on the keyboard. Check that the value changes from 00→20→80→99 and back down to 80→20→00 (in other words, apply light pressure and increase pressure to a heavier touch then decrease back to a light touch).

```
* 16: After Touch  xx  yy
```

```
* 16: After Touch  xx  yy-zz
```

(where xx=the current aftertouch value, yy and zz are the next target values)

DISPLAY OF TEST RESULTS

```
OK * 16: After Touch  00  00  OK
```

NG (No change in display message)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

17. TEST 17: MIDI TEST

```
* 17: MIDI (I/O/T)
```

After connecting the MIDI IN to the MIDI OUT via a MIDI cable, execute the test. The following message will appear on the LCD.

```
* 17: MIDI (I/O/T)  Tx:yy Rx:zz
```

TEST END

When you press [EXIT] the test will end and the SY77 will wait for a test number to be entered. If an NG error occurs, because unexpected data was received, the test will end at that point. If an NG error occurs because no data was received within a certain time, the test will continue until [EXIT] is pressed.

18. TEST 18: DATA CARD INSERT TEST

```
* 18: D-Card Insert  0
```

Insert a RAM card (MCD64) into the DATA card slot and execute the test. Check that when you remove and insert the card back into the slot, the number on the display changes from 0 to 1 and that the OK result is displayed.

DISPLAY OF TEST RESULTS

```
OK * 18: D-Card Insert  1  OK
```

NG (No change in display message)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

19. TEST 19: DATA CARDS READ/WRITE TEST

* 19: D-Card R/Write

This performs a read/write test on the following addresses of the RAM cards.

CARD 1 : 20000h-27FFFh CARD 2 : 28000h-2FFFFh

Insert a RAM cards with the memory protect turned off and execute the test.

DISPLAY OF TEST RESULTS

OK	* 19: D-Card R/Write CARD : 12	OK
----	-----------------------------------	----

NG	* 19: D-Card R/Write CARD : x	NG
----	----------------------------------	----

(e.g. if CARD 2 is No Good)

TEST END

After displaying the results, the test will end. All card data is preserved.

20. TEST 20: DATA CARD PROTECT SWITCH TEST

* 20: D-Card Protect 0

Use a RAM card to check that the card protect switch status is being read. Check that when the switch is set from "protect off" to "protect on", the number on the display changes from 0 to 1 and that the OK result is also displayed.

DISPLAY OF TEST RESULTS

OK	* 20: D-Card Protect 1	OK
----	------------------------	----

NG (No change in display)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

21. TEST 21: RAM BACKUP BATTERY TEST

* 21: D-Card Battery

This test checks that the voltage of the RAM card backup battery.

DISPLAY OF TEST RESULTS

OK	* 21: D-Card Battery #.#V	OK
----	------------------------------	----

NG	* 21: D-Card Battery #.#V Low	NG
----	-------------------------------------	----

* 21: D-Card Battery #.#V High	NG
--------------------------------------	----

TEST END

Ends after displaying the test results.

22. TEST 22: WAVEFORM CARD INSERT TEST

```
* 22: W-Card Insert 0
```

Check that when a waveform card is inserted into the slot, the number on the display changes from 0 to 1 and that the OK result is displayed.

DISPLAY OF TEST RESULTS

```
OK * 22: W-Card Insert 1 OK
```

```
NG (No change in display)
```

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

23. TEST 23: WAVEFORM CARD READ TEST

```
* 23: W-Card Read
```

This test is utilized by the factory and it is not intended for field service use.

24. TEST 24: DISK READ/WRITE TEST

```
* 24: Disk Read/Write
```

Use a blank disk to test the disk format. This test will write and read two types of data. Testing is performed on the following tracks.

SIDE 0 : TRACK 40 (sector 4)–TRACK 00 (sector 1)–TRACK 79 (sector 9)

SIDE 1 : TRACK 40 (sector 4)–TRACK 00 (sector 1)–TRACK 79 (sector 9)

Insert a blank disk with the write protect off and execute the test.

DISPLAY OF TEST RESULTS

```
OK * 24: Disk Read/Write C79:H1 Verify OK
```

```
NG * 24: Disk Read/Write Cyy:Hx nnnnnnn NG
```

(where x = side or head number, yy = track or cylinder number, and nnnnnn = condition at time of error)

TEST END

After displaying the results, the test will end.

25. TEST 25: DISK EJECT TEST

```
* 25: Disk Eject 0
```

Insert a blank disk and execute the test. Check that when the eject button is pressed and the disk is removed, the number on the display changes from 0 to 1 and that the OK result is displayed.

DISPLAY OF TEST RESULTS

OK * 25: Disk Eject 1 OK

NG (No change in display message)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

26. TEST 26: BREATH CONTROLLER TEST

* 26: Breath Control 99 00

Connect a breath controller and blow into it. Check that the number on the display changes from 00→01→20→80→95→99→80→20→01→00 (in other words, off to strong and back to off).

* 26: Breath Control xx yy-zz

(where xx = current breath control value, yy and zz are the next target values)

DISPLAY OF TEST RESULTS

OK * 26: Breath Control xx 00 OK

(where xx = breath controller value at end of test)

NG (No change in display)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

27. TEST 27: FOOT VOLUME TEST

* 27: Foot Volume 00 20-80

Connect a foot controller and operate it throughout its range. Check that the number on the display changes from 00→01→20→80→95→99→95→80→20→01→00 (in other words, starting from the raised position then to the lowered position and back to the raised position).

* 27: Foot Volume xx yy-zz

(where xx = current foot volume value, yy and zz are the next target values)

DISPLAY OF TEST RESULTS

OK * 27: Foot Volume xx 00 OK

(where xx = foot volume value at end of test)

NG (No change in display)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

28. TEST 28: FOOT CONTROLLER TEST

* 28: Foot Control	00	20-80
--------------------	----	-------

Connect a foot controller and operate it throughout its range. Check that the number on the display changes from 00→01→20→80→95→99→95→80→20→01→00 (in other words, starting from the raised position then to the lowered position and back to the raised position).

* 28: Foot Control	xx	yy-zz
--------------------	----	-------

(where xx=current foot controller value, yy and zz are the next target values)

DISPLAY OF TEST RESULTS

OK	* 28: Foot Control	xx	00	OK
----	--------------------	----	----	----

(where xx=foot controller value at end of test)

NG (No change in display)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

29. TEST 29: SUSTAIN SWITCH TEST

* 29: Sustain	1
---------------	---

Connect a sustain switch and press it on and off. Check that the number on the display changes from 1 to 0 then back to 1 and verify that the OK result is displayed.

DISPLAY OF TEST RESULTS

OK	* 29: Sustain	1	OK
----	---------------	---	----

NG (No change in display)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

30. TEST 30: FOOT SWITCH TEST

* 30: Foot Switch	1
-------------------	---

Connect a foot switch and press it on and off. Check that the number on the display changes from 1 to 0 then back to 1 and verify that the OK result is displayed.

DISPLAY OF TEST RESULTS

OK	* 30: Foot Switch	1	OK
----	-------------------	---	----

NG (No change in display)

TEST END

After displaying the result, the test will end. If NG is detected during the test, refer to section B, "B. PROCEEDING THROUGH THE TESTS".

31. TEST 31: 1 kHz FM SOUND OUTPUT (OUTPUT L1) TEST

* 31: 1KHz to L1-> L1

Check that the correct signal is output from OUTPUT L1 and PHONES (L) jacks.

The signal route is as follows:

The digital representation of the 1 kHz signal is output from S00 terminal (channel 0) of OPS3 IC (IC251) to INDV1 terminal (channel 13) of the M3 IC (IC228). From the INDV1 terminal of the M3 IC, the signal is sent to the IN1 terminal of the PAN(2) IC (IC230). From the PAN(2) IC, the signal is output from the S1 and S2 terminals. The signal is then sent to the MIX1 inputs of the MIX3 ICs (IC242 and IC243). Now the signal is sent out of the MIX3 ICs via the MXD terminals which feeds the signal to the S11 and S12 inputs of the AFDO (FLOATING POINT CONVERTER) IC. The AFDO and the DAC work together to produce the analog that is output from the CH1 (Channel 1) terminal. The signal goes to the analog circuits and is output from the OUTPUT L1 jack. It should be noted that the active low FMSEL signal must be at a 0 volt or LOW logic level in order to output this signal.

ITEMS TO CHECK

Insert the appropriate 1/4" phone plugs into each output jack and check OUTPUT L1, OUTPUT L2, OUTPUT R1, OUTPUT R2, and PHONES (L/R) outputs. If necessary, verify the frequency, output waveform, output level, and THD of each output using a frequency counter, oscilloscope, AC voltmeter (with 12.47 kHz filter) and distortion meter. The volume control must be set at maximum for these checks. While sounding, the LCD will display the following message:

* 31: 1KHz to L1-> L1 Output On

Listed below are the specifications and conditions of each output during this test.

OUTPUT L1 : 1kHz \pm 1.5Hz, sine wave, distortion 0.2%, -1.0dB \pm 2dB (10k ohm load)

OUTPUT L2 : less than -70dB

OUTPUT R1 : less than -70dB

OUTPUT R2 : less than -70dB

PHONES (L) : 1kHz, sine wave, distortion 0.2% or less, +5.0dB \pm 2dB (150 ohm load)

PHONES (R) : less than -60dB

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

* 31: 1KHz to L1-> L1 Output Off

32. TEST 32: 1kHz FM SOUND OUTPUT (OUTPUT R1) TEST

* 32: 1KHz to R1-> R1

ITEMS TO CHECK

Check that the correct signal is output from OUTPUT R1 and the PHONES (R) jacks.

The basic signal route is the same as it was in TEST 31 except the signal is output from the CH2 (Channel 2) of the AFDO IC.

Insert the appropriate 1/4" phone plugs into each output jack and check OUTPUT L1, OUTPUT L2, OUTPUT R1, OUTPUT R2, and PHONES (L/R) outputs. If necessary, verify the frequency, output waveform, output level, and THD of each output using the previously specified test equipment (refer to TEST 31). The volume control must be set at maximum for these checks. While sounding, the LCD will display the following message:

* 32: 1KHz to R1-> R1 Output On

Listed below are the specifications and conditions of each output during this test.

OUTPUT R1 : 1kHz \pm 1.5Hz, sine wave, distortion 0.2%, -1.0dB \pm 2dB (10k ohm load)

OUTPUT R2 : less than -70dB

OUTPUT L1 : less than -70dB

OUTPUT L2 : less than -70dB

PHONES (L) : less than -60dB

PHONES (R) : 1kHz, sine wave, distortion 0.2% or less, +5.0dB \pm 2dB (150 ohm load)

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

* 32: 1KHz to R1-> R1 Output Off

33. TEST 33: 1kHz FM SOUND OUTPUT (OUTPUT L2) TEST

* 33: 1KHz to L2-> L2

ITEMS TO CHECK

Check that the correct signal is output from OUTPUT L2 and the PHONES (L) jacks.

The basic signal route is the same as it was in TEST 31 except the signal is output from the CH3 (Channel 3) of the AFDO IC.

Insert the appropriate 1/4" phone plugs into each output jack and check OUTPUT L1, OUTPUT L2, OUTPUT R1, OUTPUT R2, and PHONES (L/R) outputs. If necessary, verify the frequency, output waveform, output level, and THD of each output using the previously specified test equipment (refer to TEST 31). The volume control must be set at maximum for these checks. While sounding, the LCD will display the following message:

* 33: 1KHz to L2-> L2 Output On

Listed below are the specifications and conditions of the output during this test.

OUTPUT L2 : 1kHz \pm 1.5Hz, sine wave, distortion 0.2%, -1.0dB \pm 2dB (10k ohm load)

OUTPUT L1 : less than -70dB

OUTPUT R1 : less than -70dB

OUTPUT R2 : less than -70dB

PHONES (L) : 1kHz, sine wave, distortion 0.2% or less, +5.0dB \pm 2dB (150 ohm load)

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

* 33: 1KHz to L2-> L2 Output Off

34. TEST 34: 1kHz FM SOUND OUTPUT (OUTPUT R2) TEST

* 34: 1KHz to R2-> R2

ITEMS TO CHECK

Check that the correct signal is output from OUTPUT R2 and the PHONES (R) jacks.

The basic signal route is the same as it was in TEST 31 except the signal is output from the CH4 (Channel 4) of the AFDO IC.

Insert the appropriate 1/4" phone plugs into each output jack and check OUTPUT L1, OUTPUT L2, OUTPUT R1, OUTPUT R2, and PHONES (L/R) outputs. If necessary, verify the frequency, output waveform, output level, and THD of each output using the previously specified test equipment (refer

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to TEST 31). The volume control must be set at maximum for these checks. While sounding, the LCD will display the following message:

* 34: 1KHz to R2-> R2 Output On

Listed below are the specifications and conditions of each output during this test.

OUTPUT R2 : 1kHz \pm 1.5Hz, sine wave, distortion 0.2%, - 1.0dB \pm 2dB (10k ohm load)

OUTPUT R1 : less than -70dB

OUTPUT L1 : less than -70dB

OUTPUT L2 : less than -70dB

PHONES (R) : 1kHz, sine wave, distortion 0.2% or less, + 5.0dB \pm 2dB (150 ohm load)

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

* 34: 1KHz to R2-> R2 Output Off

35. TEST 35: 1kHz FM SOUND OUTPUT (OUTPUT L2 OUTPUT L1) TEST

* 35: 1KHz to L2-> L1

ITEMS TO CHECK

Check that when the plug connected to OUTPUT L2 is pulled out, the signal being output from OUTPUT L2 is now output from OUTPUT L1. The basic signal route is the same as it was for TEST 33.

Insert the appropriate 1/4" phone plug into OUTPUT L1 and verify, if necessary, the frequency, output waveform, output level, and THD of this output using the previously specified test equipment (refer to TEST 31). The volume control must be set at maximum for this test. While sounding, the LCD will display the following message:

* 35: 1KHz to L2-> L1 Output On

The specifications for this test are as follows:

OUTPUT L1 : 1kHz, sine wave, - 1.0dB \pm 2dB (10k ohm load)

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

* 35: 1KHz to L2-> L1 Output Off

36. TEST 36: 1kHz FM SOUND OUTPUT (OUTPUT R2 OUTPUT R1) TEST

* 36: 1KHz to R2-> R1

ITEMS TO CHECK

Check that when the plug connected to OUTPUT R2 is pulled out, the signal being output from OUTPUT R2 is now output from OUTPUT R1. The basic signal route is the same as it was for TEST 34.

Insert the appropriate 1/4" phone plug into OUTPUT R1 and verify, if necessary, the frequency, output waveform, output level, and THD of this output using the previously specified test equipment (refer to TEST 31). The volume control must be set at maximum for this test. While sounding, the LCD will display the following message:

* 36: 1KHz to R2-> R1 Output Off

The specifications for this test are as follows:

OUTPUT R1 : 1kHz, sine wave, $-1.0\text{dB} \pm 2\text{dB}$ (10k ohm load)

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

* 36: 1KHz to R2-> R1 Output Off

37. TEST 37: 1kHz FM SOUND OUTPUT (OUTPUT R1→OUTPUT L1) TEST

* 37: 1KHz to R1-> L1

ITEMS TO CHECK

Check that when the plug connected to OUTPUT R1 is pulled out, the signal being output from OUTPUT R1 is now output from OUTPUT L1. The basic signal route is the same as it was for TEST 32.

Insert the appropriate 1/4" phone plug into OUTPUT L1 and verify, if necessary, the frequency, output waveform, output level, and THD of this output using the previously specified test equipment (refer to TEST 31). The volume control must be set at maximum for this test. While sounding, the LCD will display the following message:

* 37: 1KHz to R1-> L1 Output On

The specifications for this test are as follows:

OUTPUT L1 : 1kHz, sine wave, $-1.0\text{dB} \pm 2\text{dB}$ (10k ohm load)

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

* 37: 1KHz to R1-> L1 Output Off

38. TEST 38: 1kHz FM SOUND OUTPUT (EFFECT 0→OUTPUT L1) TEST

* 38: Effect_0 to L1

ITEMS TO CHECK

The basic signal route is the same as it was for TEST 31 except that the signal is sent out of CH1 through CH4 (Channels 1–4). In other words, a signal is output to OUTPUT L1, OUTPUT L2, OUTPUT R1 and OUTPUT R2. With no 1/4" phone plugs inserted, the signals from these outputs will all be sent to OUTPUT L1.

Insert the appropriate 1/4" phone plug into OUTPUT L1 only and verify, if necessary, the frequency, output waveform, output level, and THD of this output using the previously specified test equipment (refer to TEST 31).

The volume control must be set at maximum for this test. While sounding, the LCD will display the following message:

* 38: Effect_0 to L1 Output On

The specifications for this test are as follows:

OUTPUT L1 : 1kHz, sine wave, distortion 0.3% or less, $+11.0\text{dB} \pm 2\text{dB}$ (10k ohm load)

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TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;
(1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

```
* 38: Effect_0 to L1 Output Off
```

39. TEST 39: 1kHz FM SOUND OUTPUT (EFFECT 1→OUTPUT L1) TEST

```
* 39: Effect_1 to L1
```

There are two signal paths for this test. The basic signal path is the same as it was for TEST 31 except for the following:

SIGNAL PATH 1

The signal from the PAN IC is input to pin 2 (SIO terminal) of the LEF (1) IC (IC232) via pin 9 of IC254. The signal is then output from pin 4 (SOO terminal) of the LEF (1) IC to pin 10 (SIO terminal) of the LDSP (1) IC (IC236).

The LDSP(1) IC outputs the signal via pin 33 (SOO terminal) to pin 2 (MIX2 terminal) of MIX3 (1) IC (IC242). This ultimately produces signal output from OUTPUT L1 and OUTPUT R1.

SIGNAL PATH 2

The signal from the PAN IC is input to pin 2 (SIO terminal) of the LEF (2) IC (IC233) via pin 19 of IC254. The signal is then output from pin 4 (SOO terminal) of the LEF (2) IC to pin 10 (SIO terminal) of the LDSP (2) IC (IC237). The LDSP (2) IC outputs the signal via pin 33 (SOO terminal) to pin 2 (MIX2 terminal) of MIX3 (2) IC (IC243). This ultimately produces signal output from OUTPUT L2 and OUTPUT R2.

It should be noted that the LEF ICs use their associated DRAM ICs and the LDSP ICs use their associated PSRAM to process the signals for this test.

ITEMS TO CHECK

Insert the appropriate 1/4" phone plug into OUTPUT L1 only and verify, if necessary, the frequency, output waveform, output level, and THD of this output using the previously specified test equipment (refer to TEST 31). The volume control must be set at maximum for this test.

While sounding, the LCD will display the following message:

```
* 39: Effect_1 to L1 Output On
```

The specifications for this test are as follows:

OUTPUT L1 : 1kHz, sine wave, distortion 0.3% or less, +11.0dB±2dB (10k ohm load)

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;
(1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

```
* 39: Effect_1 to L1 Output Off
```

40. TEST 40: 1kHz FM SOUND OUTPUT (EFFECT 2→OUTPUT L1) TEST

```
* 40: Effect-2 to L1
```

There are two signal paths for this test. The basic signal path is the same as it was for TEST 31 except for the following:

SIGNAL PATH 1

The signal from the PAN IC is input to pin 2 (SIO terminal) of the LEF (2) IC (IC233) via pin 19 of IC254. The signal is then output from pin 4 (SOO terminal) of the LEF (2) IC to pin 11 (SI1 terminal) of the LDSP (1) IC (IC236). The LDSP (1) IC outputs the signal via pin 33 (SOO terminal) to pin

11 (S11 terminal) of the LDSP (2) IC (IC237). From the LDSP (2) IC, pin 33 (SO0 terminal), the signal is output to pin 3 (MIX3 terminal) of MIX3 (1) IC (IC242). This ultimately produces signal output from OUTPUT L1 and OUTPUT R1.

SIGNAL PATH 2

The signal from the PAN IC is input to pin 2 (S10 terminal) of the LEF (2) IC (IC233) via pin 19 of IC254. The signal is then output from pin 5 (SO1 terminal) of the LEF (2) IC to pin 4 (MIX4 terminal) of MIX3 (2) IC (IC243). This ultimately produces signal output from OUTPUT L2 and OUTPUT R2.

It should be noted that the LEF ICs use their associated DRAM ICs and the LDSP ICs use their associated PSRAM to process the signals for this test.

ITEMS TO CHECK

Insert the appropriate 1/4" phone plug into OUTPUT L1 only and verify, if necessary, the frequency, output waveform, output level, and THD of this output using the previously specified test equipment (refer to TEST 31). The volume control must be set at maximum for this test.

While sounding, the LCD will display the following message:

```
* 40: Effect-2 to L1 Output On
```

The specifications for this test are as follows:

OUTPUT L1 : 1kHz, sine wave, distortion 0.3% or less, +10.0dB±2dB (10k ohm load)

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

```
* 40: Effect-2 to L1 Output Off
```

41. TEST 41: AWM (M3) SOUND OUTPUT TEST

```
* 41: PCM Check
```

SIGNAL PATH

This outputs the sound which is stored in addresses 012000h–01FFFFh of WAVE ROM. The data stored at these addresses is retrieved by the M3(A) IC (IC205) and output via pin 1 (INDV0 terminal, channel 0). The signal from pin 1 is then output to pin 11 (INO terminal) of the PAN(1) IC (IC229). The PAN (1) IC outputs the signal from pins 21 and 22 (S1 and S2 terminals, respectively) and sends the signal to pins 12 and 13 (S12 and S11 terminals, respectively) of the PAN (2) IC (IC230). The PAN (2) IC outputs the signal from pins 21 and 22 (S1 and S2 terminals, respectively) to pin 1 (MIX1 terminal) of each MIX3 IC. This ultimately produces signal output from OUTPUT L1, OUTPUT R1, OUTPUT L2, OUTPUT R2.

ITEMS TO CHECK

Confirm that a AWM signal is being sent to OUTPUT L1 using an amplifier and speaker to monitor the signal. The AWM signal is not a steady tone. While this signal is sounding, the LCD will display the following message:

```
* 41: PCM Check      Output On
```

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur;

(1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

```
* 41: PCM Check      Output Off
```

42. TEST 42: FM SOUND OUTPUT THROUGH M3 IC (AWM) TEST

* 42: FM Thru M3(PCM)

SIGNAL PATH

A sine wave which is frequency swept by the EGM2 (1) IC will cause signals to be alternately output from OUTPUT L1, OUTPUT R1, OUTPUT L2 and OUTPUT R2 in a two channel pair sequence. The FMSEL signal to the EGM2 (1) and OPS3 (1) must be at a 1 or HIGH logic level for this test. The appropriate data from EGM2 (1) IC (IC226) is sent to the OPS3 (1) IC (IC227) in order to produce the sound. The OPS3 (1) IC outputs the signals from pins 54 and 55 (SO0, channel 1 and SO1, channel 9) via IC252 (pins 3 and 6) to pins 27 and 28 (terminals DIINO and DIIN1) of the M3 (A) IC (IC205). The M3 (A) IC outputs the signals from pins 1 and 2 (INDV0, channel 5 and INDV1, channel 6) to pins 10 and 11 (IN1 and IN0 terminals) of the PAN (1) IC (IC229). The PAN (1) IC sends the signals out from pins 21 and 22 (S1 and S2 terminals) to pins 12 and 13 (SI2 and SI1 terminals) of the PAN (2) IC (IC230). The PAN (2) IC outputs the signals from pins 21 and 22 (S1 and S2 terminals) to pin 1 (MIX1 terminal) of each MIX3 IC. This ultimately produces signal output from OUTPUT L1, OUTPUT R1, OUTPUT L2, OUTPUT R2.

ITEMS TO CHECK

Insert the appropriate 1/4" phone plug into OUTPUT L1 and observe the output waveform with an oscilloscope. Check that the level does not change excessively as the output sweeps through its frequency range. The volume control must be set at comfortable listening level for this test. While sounding, the LCD will display the following message.

* 42: FM Thru M3(PCM) Output On

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur; (1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

* 42: FM Thru M3(PCM) Output Off

43. TEST 43: FM SOUND OUTPUT THROUGH M3 IC (DIGITAL FILTER) TEST

* 43: FM Thru M3(FM)

SIGNAL PATH

A sine wave which is frequency swept by the EGM2 (2) IC will cause signals to be alternately output from OUTPUT L1, OUTPUT R1, OUTPUT L2 and OUTPUT R2 in a two channel pair sequence. The FMSEL signal to the EGM2 (2) and OPS3 (2) must be at a 0 or LOW logic level for this test. The appropriate data from EGM2 (2) IC (IC250) is sent to the OPS3 (2) IC (IC251) in order to produce the sound. The OPS3 (2) IC outputs the signals from pins 54 and 55 (SO0, channel 0 and SO1, channel 8) via IC252 (pins 3 and 6) to pins 27 and 28 (terminals DIINO and DIIN1) of the M3 (B) IC (IC228). The M3 (B) IC outputs the signals from pins 1 and 2 (INDV0, channel 14 and INDV1, channel 15) to pins 10 and 11 (IN1 and IN0 terminals) of the PAN (2) IC (IC230). The PAN (2) IC sends the signals out from pins 21 and 22 (S1 and S2 terminals) to pin 1 (MIX1 terminal) of each MIX3 IC. This ultimately produces signal output from OUTPUT L1, OUTPUT R1, OUTPUT L2, OUTPUT R2.

ITEMS TO CHECK

Insert the appropriate 1/4" phone plug into OUTPUT L1 and observe the output waveform with an oscilloscope. Check that the level does not change excessively as the output sweeps through its frequency range. The volume control must be set at a comfortable listening level for this test. While sounding, the LCD will display the following message.

* 43: FM Thru M3(FM) Output On

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur; (1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

* 43: FM Thru M3(FM) Output Off

44. TEST 44: FM SOUND OUTPUT FEEDBACK THROUGH M3 IC TEST

* 44: Feedback FM->M3

The basic signal path is the same as it was for TEST 42 except for the following: The frequency swept sine wave produced by the EGM2 (1) and OPS3 (1) will be fed back from the M3 (A) IC to the OPS3 (1) IC. As in TEST 42, the output signals will occur alternately in a two channel pair sequence. For this test, the signals from pins 1 and 2 (INDV0 and INDV1 terminals) of M3 (A) IC (IC205) will be fed back to pins 69 and 70 (S10 and S11 terminals) of OPS3 (1) IC (IC227).

ITEMS TO CHECK

Insert the appropriate 1/4" phone plug into OUTPUT L1 and observe the output waveform with an oscilloscope. Check that the level does not change excessively as the output sweeps through its frequency range. It should be noted that due to the feedback condition of this test there may be a slight amount of distortion present in the output signal. The volume control must be set at a comfortable listening level for this test. While sounding, the LCD will display the following message:

* 44: Feedback FM->M3 Output On

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur; (1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

* 44: Feedback FM Output Off

45. TEST 45: HIGH CLICK SOUND TEST

* 45: Click High

ITEMS TO CHECK

Check that a high click signal is properly output from OUTPUT L1, OUTPUT L2, OUTPUT R1 and OUTPUT R2. Make sure that the click volume control is set to maximum. While sounding, the LCD will display the following message:

* 45: Click High Click On

Verify that the high click signal is sent to each output by using an amplifier and speaker to monitor signal. Insert the appropriate 1/4" phone plugs into OUTPUT L1, OUTPUT L2, OUTPUT R1 and OUTPUT R2 and observe the output waveform with an oscilloscope. Check that the output waveform is a rounded square wave with an approximate peak-to-peak voltage of 500mV.

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur; (1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

* 45: Click High Click Off

46. TEST 46: LOW CLICK SOUND TEST

* 46: Click Low

ITEMS TO CHECK

Check that a low click signal is properly output from OUTPUT L1. Make sure that the click volume control is set to maximum. While sounding, the LCD will display the following message:

* 46: Click Low	Click On
-----------------	----------

Verify that the low click signal is sent to OUTPUT L1 by using an amplifier and speaker to monitor signal. Insert the appropriate 1/4" phone plugs into OUTPUT L1, OUTPUT L2, OUTPUT R1 and OUTPUT R2 and observe the output waveform with an oscilloscope. Check that the output waveform is a rounded square wave with an approximate peak-to-peak voltage of 500mV.

TEST END

Press [EXIT] to end the test. After pressing [EXIT] three things occur; (1) the following display will appear, (2) the sound will stop and (3) the SY77 will wait for the entry of a test number.

* 46: Click Low	Click Off
-----------------	-----------

47. TEST 47: JACKS ALL OFF TEST

* 47: Jack All Off

Connect the Sustain and Foot Switch pedals to the appropriate jacks. With nothing connected to the Foot Volume, Foot Controller, and Breath controller jacks, check that the following display appears.

* 47: Jack All Off	SU FS
--------------------	-------

Then while pressing the foot switches connected to the Sustain and Foot Switch jacks, remove the pedal plugs, and check that the display shows "OK".

DISPLAY OF TEST RESULTS

OK	* 47: Jack All Off	OK
----	--------------------	----

NG	* 47: Jack All Off	FV	NG
----	--------------------	----	----

(e.g. if the foot volume jack is NG)

TEST END

The result is displayed and the test will end.

48. TEST 48: FACTORY SET TEST

* 48: Factory Set

This test is used to initialize the data listed below to the factory settings:

Synthesizer system data
64-internal voice data
16-internal multi data
Sequencer setup data

When this test is executed, the following display will appear.

```
* 48: Factory Set [NO] or [YES] ?
```

If you press [YES], the factory preset data will be restored.
If you press [NO], they will not be restored.

DISPLAY OF TEST RESULTS

If factory settings are restored.

```
OK * 48: Factory Set OK
```

If not restored there will be no change in the display as shown below.

```
* 48: Factory Set [NO] or [YES] ?
```

TEST END

The LCD displays the results, the factory preset data will be restored, and the test will then end.
After the factory preset data has been restored, the system data will be as follows:

```
*****
*      SYNTH      *
*****
```

```
Note Shift.....+0
Fine Turning .....+0
Fixed Velocity.....off
Velocity Curve .....0(normal)
Assignable Foot Switch .....65
Assignable Wheel .....13
Edit Confirm .....on
Kbd Trans Ch .....1
Voice Recv Ch.....omn
Local on/off.....on
Note on/off .....all
Device Number .....all
Bulk Protect .....on
Program Change.....normal
```

----- Greeting Message -----

```
"Create YOUR sound!"
"...I'm ready"
```

----- PAN factory set -----

```
11~132 = P1 ~P32
```

----- MCT factory set -----

```
I 1 = P62(Far East)
I 2 = P63(Blue)
```

----- VOICE -----

```
I-A01~D16 =P1-A01~D16
```

----- MULTI -----

```
I-A01~D16 =P1-A01~D16
```


SY77

SY77

```
*****
*   SEQUENCER   *
*****
record quantize .....0(off)
click sw .....1(rec)
click beat .....0(1/4)

record type .....over
sync .....0(internal)
receive .....KBD

filter velocity .....1(on)
filter control change .....1(on)
filter pitch bend .....1(on)
filter program change .....0(off)
filter after touch .....0(off)
filter exclusive .....1(on)

midi control .....1(on)
click/beat .....1/96

accent 1 value .....24
accent 2 value .....56
accent 3 value .....88
accent 4 value .....120
gate type .....1(normal)
```

49. TEST 49: EXIT TEST PROGRAM

* 49: Exit

When this is executed, the following display will appear.

* 49: Exit [NO] or [YES] ?

To exit the test program mode, press the [YES] switch. To remain in the test program mode press the [NO] switch. This will cause the SY77 to wait for the entry of a test number.

DISPLAY OF TEST RESULTS

If test mode is not exited.

* 49: Exit [NO] or [YES] ?

MUSIC SYNTHESIZER
SY77
PARTS LIST

Notes DESTINATION ABBREVIATIONS

J : Japanese model	A : Australian model
U : U.S. model	E : European model
C : Canadian model	D : West German model
X : General model	B : British model
M : South African model	I : Indonesian model
H : North European model	

SY77

ELECTRICAL PARTS (電気部品)

Ref. No.	Part No.	Description	部品名	Remarks	ランク
	VH799000	Circuit Board	DM1	DM1シート	
	VH799100	Circuit Board	DM2	DM2シート	
	VH799200	Circuit Board	PNAB	PNABシート	
	VH799400	Circuit Board	PNC	PNCシート	
	NX808420	Circuit Board	JKAN	JKANシート	
	NX808430	Circuit Board	CARD	CARDシート	
	NA115670	Circuit Board	MK	MKシート	09
	NA109720	Circuit Board	PC	PCシート	07
	VH799600	Circuit Board	PS	PSシート	J
	VH799700	Circuit Board	PS	PSシート	U.C
	VH799800	Circuit Board	PS	PSシート	H,D,A,B
	VH799000	Circuit Board	DM1	DM1シート	
	IG001390	IC	RC4558D-V	IC	OP AMP.
	IG116200	IC	PST518B-2	IC	SYSTEM RESET
	IG063690	IC	74F00PC	IC	NAND
	IR000250	IC	SN74HC02N	IC	NOR
	IG027020	IC	SN74LS04N	IC	INVERTER
	IG142250	IC	SN74HC04N	IC	INVERTER
	XC723001	IC	SN74HC04NSR	IC	INV. S/#PZ1001-
	XA876001	IC	SN74ALS08N	IC	AND
	IR001450	IC	SN74HC14N	IC	INVERTER
	IG058990	IC	74F32PC	IC	OR
	IR003250	IC	SN74HC32N	IC	OR
	XA055001	IC	SN74ALS32N	IC	OR
	IR007450	IC	SN74HC74N	IC	D-FF
	XA196A00	IC	SN74ALS74N	IC	FF
	IG120090	IC	74F138PC	IC	3-8DECODER
	IG149600	IC	SN74ALS138N	IC	DECODER
	IR013850	IC	SN74HC138N	IC	3-8DECODER
	IG149900	IC	SN74ALS245AN	IC	BUS TRANSCEIVER
	IR024500	IC	TC74HC245P	IC	BUS BUFFER
	IG115300	IC	HD74LS670P	IC	REGISTER FILE
	IR405200	IC	TC74HC4052AP	IC	DEMULTIPLXER
	XF148A00	IC	HD63C01Y0F64P	IC	SEQ. CPU
	XG944B00	IC	HD6475328CP-10	IC	MAIN CPU H8/532
	XG950B00	IC	HD637B01Y	IC	CPU-PKS
	XB361001	IC	μ PD71055C	IC	PPI
	XH129A00	IC	WD37C65B-JM00	IC	FDC
	XF876A00	IC	LH5164D-10L	IC	SRAM 64K
	XF863A00	IC	μ PD43256AC-12L	IC	SRAM 256K
	XG708A00	IC	HM62256LP-12	IC	SRAM 256K
	XG960A00	IC	TC55257BPL-10	IC	SRAM 256K
	XC628A00	IC	TC51832PL-10	IC	PSRAM 256K
	XH116A00	IC	HM65256BPL-10	IC	PSRAM 256K
	XH118B00	IC	101AV100 12nsec	IC	EPROM V1.00
	XH119B00	IC	101BV100	IC	EPROM V1.00
	XH120B00	IC	120nsec 101CV100	IC	EPROM V1.00
	XH121B00	IC	101DV100	IC	EPROM V1.00
	XH122B00	IC	120nsec 101EV100	IC	EPROM V1.00
	IA101521	Transistor	2SA1015 Y	トランジスタ	03
	IC181520	Transistor	2SC1815 Y	トランジスタ	03
	IF003450	Diode	1SS133	ダイオード	01
	V1546800	Zener Diode	RD3.0ESB1 3V	ツェナーダイオード	01
	U1838470	Electrolytic Cap.	470 μ 16V M	ケミコン	01
	FP736470	Tantalum Capacitor	4.7 μ 16V M	タンタルコン	01
	VC694800	Semiconductive Cera. Cap.	0.1 μ 25V Z	半導体セラコン	01
	VC824900	Metal Film Resistor	10K Ω 1/6W F	金属膜抵抗	01
	H2004650	Resistor Array	RMLS6J103	抵抗アレイ	02
	VA822600	Resistor Array	RMLS4J103	抵抗アレイ	01
	VE445200	Resistor Array	RGLD8X103J	抵抗アレイ	01
	VE445300	Resistor Array	RGLD8X153J	抵抗アレイ	01
	VE445400	Resistor Array	RGLD8X223J	抵抗アレイ	01
	V1635300	Resistor Array	RMLS6-221J	抵抗アレイ	01
	FZ006970	EMI Filter	LS MT Y223NB	L.C.フィルター EMI	02
	VE463500	Quartz Crystal Unit	AT-49 12MHz	水晶振動子	03
	V1927300	Quartz Crystal Unit	AT-49 20MHz	水晶振動子	03
	V1927400	Quartz Crystal Unit	DOC-492 16MHz	水晶振動子	S/# PY1001-2220
	V1573400	Quartz Crystal Unit	AT-49 16MHz	水晶振動子	S/# PZ1001-
	VE338400	Lithium Battery	SONY/CR2032	リチウム電池	03
	VH930600	Angle Bracket, Earth		アース金具	01
	VH799100	Circuit Board	DM2	DM2シート	
	XD830A00	IC	SN74HC04NSR	IC	INVERTER
	IG049850	IC	SN74LS32N	IC	OR

1

* New Parts (新規部品)

ランク: Japan only

SY77

Ref. No.	Part No.	Description	部品名	Remarks	ランク	
	IR013950	IC	SN74HC139N	I C	2-4DECODER	05
	IG044600	IC	SN74LS245	I C	TRANSCEIVER	08
	IG149900	IC	SN74ALS245AN	I C	BUS TRANSCEIVER	07
	IR024550	IC	SN74HC245N	I C	TRANSCEIVER	06
	IR027350	IC	SN74HC273N	I C	D-FF OCTAL	05
	IR036750	IC	SN74HC367N	I C	BUS DRIVER	06
	IG156010	IC		I C	MIX3	05
	XE449A00	IC	YM3413	I C	LDSP	10
	XE450A00	IC	YM3415	I C	LEF	12
	XG996A00	IC	YM7102	I C	PAN	10
	XG993A00	IC	YM7103	I C	EGM2	13
	XG994A00	IC	YM7107	I C	OPS3	13
	XG995A00	IC	YM7119	I C	M3	18
	XD281A00	IC	LM2464-12	I C	DRAM 256K	08
	XC628A00	IC	TC51832PL-10	I C	PSRAM 256K	09
	XH116A00	IC	NH652568LP-10	I C	PSRAM 256K	09
	XH024B00	IC	NH62304BPH28	I C	ROM-A 4M	16
	XH025B00	IC	NH62304BPH29	I C	ROM-B 4M	16
	XH026B00	IC	NH62304BPH30	I C	ROM-C 4M	16
	XH027B00	IC	NH62304BPH31	I C	ROM-D 4M	16
	XH028B00	IC	NH62304BPH32	I C	ROM-E 4M	16
	XH029B00	IC	NH62304BPH33	I C	ROM-F 4M	16
	XH030B00	IC	NH62304BPH34	I C	ROM-G 4M	16
	XH031B00	IC	NH62304BPH35	I C	ROM-H 4M	16
	VC694800	Semiconductive Cera. Cap.	0.1μ 25V Z	半導体セラコン		01
	VE443500	Resistor Array	RGLD4X103J	抵抗アレイ		01
	VE445200	Resistor Array	RGLD8X103J	抵抗アレイ		01
	FZ006970	EMI Filter	LS MT Y223NB	L C フィルター E M I		02
	VH949900	Quartz Crystal Unit	AT-49 6.144MHz	水晶振動子		03
	VH930600	Angle Bracket, Earth		アース金具		01
	VH799200	Circuit Board	PNAB	P N A B シート		03
	IA101521	Transistor	2SA1015 Y	トランジスタ		01
	VG197400	LED	GL3HD18 RE	L E D	UTI, BYPASS, RECO	01
	VG197600	LED	GL3ED8 RE+GR	2色 L E D	MODE, RUN (5pcs)	01
	VE373500	Slide Pot.	A10K X 2	二選スライドボリューム	VOL. (OUTPUT1,2)	03
	VF946200	Push Switch	SOA-111HS	プッシュスイッチ	(25pcs)	01
	VH812000	LED Spacer	× 8	L E D スペース	LED1-6	02
	VH812100	LED Spacer	× 4	L E D スペース	LED7,8	01
	VH799400	Circuit Board	PNC	P N C シート		05
	IR027350	IC	SN74HC273N	I C	D-FF OCTAL	01
	IF003450	Diode	1SS133	ダイオード		01
	VG197400	LED	GL3HD18 RE	L E D	MEMORY, BANK (8pc)	01
	VG197600	LED	GL3ED8 RE+GR	2色 L E D	Voice sel.1-16	01
	VC694800	Semiconductive Cera. Cap	0.1μ 25V Z	半導体セラコン		01
	VC250600	Slide Pot.	B10K EWA-NPOC	スライドボリューム	DATA ENTRY	03
	VB436400	Rotary Switch	EC24B30D	ロータリースイッチ	Data entry Dial	07
	VF946200	Push Switch	SOA-111HS	プッシュスイッチ	(45pcs)	01
	VH812000	LED Spacer	× 8	L E D スペース		02
	NX808420	Circuit Board	JKAN	J K A N シート		03
	IG001390	IC	RC4558D-V	I C	OP AMP.	04
	IG042500	IC	NJM4556	I C	OP AMP.	04
	XA013001	IC	M5238P	I C	OP AMP.	04
	IG130500	IC	NJW79L05	I C	REGULATOR -5V	03
	XC349001	IC	μ PC78L05J	I C	REGULATOR +5V	02
	IG043300	IC	TC4093BP	I C	NAND	05
	IG052600	IC	HD74LS05P	I C	INVERTER	03
	XB637001	IC	PCM56P	I C	DA CONVERTER	09
	XF237A00	IC	YH3020	I C	AFDO	09
	VD473200	Photo Coupler	6N137	フォトカプラ		05
	IA111510	Transistor	2SA1115 E,F	トランジスタ		03
	IC094530	Transistor	2SC945A PA	トランジスタ		03
	IC260320	Transistor	2SC2603 E,F	トランジスタ		03
	IC287820	Transistor	2SC2878 A,B	トランジスタ		03
	IF003450	Diode	1SS133	ダイオード		01
	VC694800	Semiconductive Cera. Cap.	0.1μ 25V Z	半導体セラコン		01
	VG582600	DC/AC Inverter Transformer	D32-49	D C / A C インバータトランス		07
	VB835000	Coil	20μ H FL5R200QN	コイル		01
	VD048800	Variable Resistor	A10K EVU-E	ロータリーボリューム	CLICK VOLUME	02
	V1573700	Variable Resistor	BLK EVU-E2A	ロータリーボリューム	CONTRAST	02
	LB203090	Phone Jack	HLJ0521 STEREO	ホンジャック	PHONES	02
	LB301780	Phone Jack	HLJ4306 STEREO	ホンジャック	OUTPUT1/1+2(R)	03
	LB302010	Phone Jack	HSJ0912 ST-Mini	ホンジャック	BREATH	02
	VE742000	Phone Jack	HLJ4306 MONO.	ホンジャック	F. SW. SUS. OUT1(L)	02
	VE742200	Phone Jack	HLJ4306 STEREO	ホンジャック	F. VOLUME, F. CONT	02
	VI662400	Phone Jack	HLJ4306 STEREO	ホンジャック	OUTPUT2(L/R)	02
	LB500520	DIN Jack	5P TCS4650	D I N ジャック	MIDI(IN,OUT,THR)	03

* New Parts (新規部品)

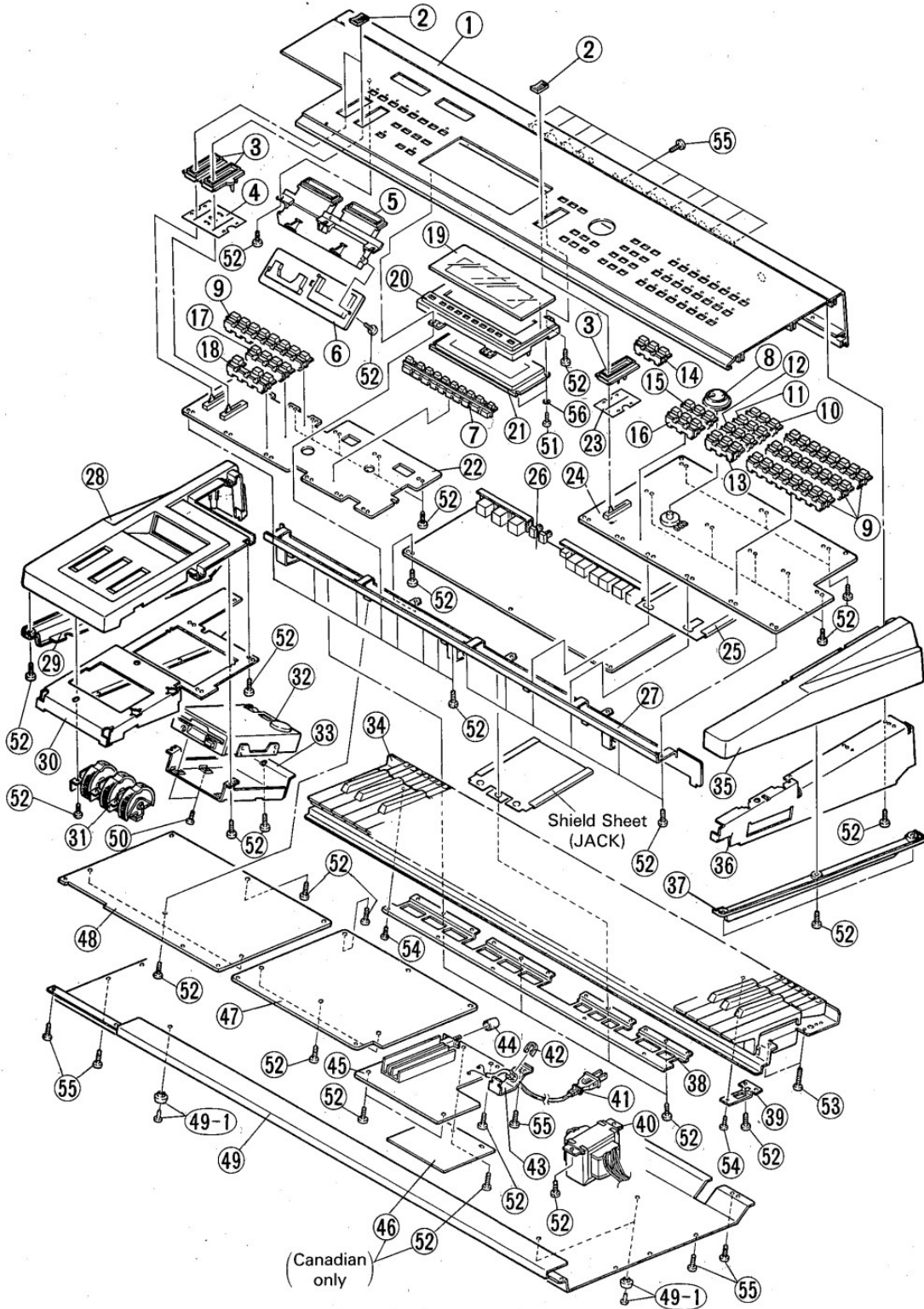
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Ref. No.	Part No.	Description	部品名	Remarks	ランク
**	VH812200	Angle Bracket-H,Jack	J K アングル (H)	JK1-10(OUT-BRE	03
**	VH812300	Angle Bracket-M,Jack	J K アングル (M)	JK12-14(MIDI)	02
**	NX808430	Circuit Board	CARD	C A R D シート	01
**	VC694800	Semiconductive Cera. Cap.	0.1 μ 25V Z	半導体セラコン	01
**	VF821100	Connector, IC Card	38P	I C カード用コネクタ	DATA
**	VH985300	Connector, IC Card	50P	I C カード用コネクタ	WAVEFORM
**	NA115670	Circuit Board	MK	M K シート	09
**	IF003450	Diode	1SS133	ダイオード	01
**	NA109720	Circuit Board	PC	P C シート	07
**	IG001390	IC	RC4558D-V	I C	OP AMP
**	IC232040	Transistor	2SC2320 F	トランジスタ	03
**	IF000040	Diode	1S1555	ダイオード	01
**	VJ602000	Zener Diode	05A25.1V 5.1V	ツェナーダイオード	01
**	HT370250	Trimmer Potentiometer	B50K 3P	半固定抵抗	Offset adjust
**	HT370260	Trimmer Potentiometer	B100K 3P	半固定抵抗	Gain adjust
**	VH799600	Circuit Board	PS	P S シート	J
**	VH799700	Circuit Board	PS	P S シート	U,C
**	VH799800	Circuit Board	PS	P S シート	H,D,A,B
**	IG136200	IC	SC-3052V	I C	+5V 2A
**	XD340001	IC	AN78M12F	I C	REGULATOR +12V
**	XD342001	IC	AN79M12F	I C	REGULATOR -12V
**	IF990300	Diode Stack	S5VB20 3.5A200V	ダイオードスタック	08
**	VD488400	Diode Stack	RDF04M 1A 400V	ダイオードスタック	02
**	IF008900	Zener Diode	MTZ13C 13V	ツェナーダイオード	01
**	U1949100	Electrolytic Cap.	1000 μ 25V	ケミコン	02
**	U1949220	Electrolytic Cap.	2200 μ 25V	ケミコン	03
**	UJ63A100	Electrolytic Cap.	10000 μ 16V	ケミコン	04
**	FI383220	Ceramic Cap.	2200P 400V	規格認定コン	01
**	FI383470	Ceramic Cap.	4700P 400V	規格認定コン	H,D,A,B
**	FI494100	Ceramic Cap.	0.01 μ 400V	規格認定コン	01
**	VC694800	Semiconductive Cera. Cap.	0.1 μ 25V Z	半導体セラコン	01
**	GD900760	Coil	3mH PLA3021A	コイル	06
**	VF576000	Push Switch	ESB-8236V JUCS	プッシュスイッチ	POWER
**	KB000310	Fuse	T 500mA 250V	ヒューズ	J
**	KB000330	Fuse	T 1A 250V	ヒューズ	01
**	KB000360	Fuse	T 3A 250V	ヒューズ	J
**	KB001150	Fuse	T 500mA 250V	ヒューズ	U,C
**	KB001060	Fuse	T 1A 250V	ヒューズ	U,C
**	KB002650	Fuse	T 3A 250V	ヒューズ	U,C
**	KB000710	Fuse	T 500mA 250V	ヒューズ	H,D,A,B
**	KB000760	Fuse	T 3.15A 250V	ヒューズ	H,D,A,B
**	KB001770	Fuse	T 1A 250V	ヒューズ	H,D,A,B
**	LB201530	Fuse Holder	PC-FH1	ヒューズホルダー	02
**	IL000680	Insulation Sheet	BFG-20	放熱シート	01
**	E1030106	Bind Head Tapping Screw	3.0 \times 10 ZMC2Y	ハットタッピングネジ	(5pcs)
**	VG782900	Floppy Disk Drive Unit	D357B 3.5inch	F D ドライブユニット	26
**	VE469300	Variable Resistor	10K RK1241110	ロータリーポリウム	PITCH BEND
**	NS412160	Variable Resistor	10K K161100S	ロータリーポリウム	MODULATION 1
**	VI666700	Variable Resistor	10K RK1631110	ロータリーポリウム	MODULATION 2
**	VF931200	LCD	DMF-5005N	液晶ディスプレイ	28
**	VD279200	AC Cord	7A 2.5m	電源コード	J
**	VD279400	AC Cord	10A 2.5m	電源コード	U
**	VD279500	AC Cord	10A 2.5m	電源コード	C
**	VD280400	AC Cord	2.5A 2.5m	電源コード	H,D
**	VD279700	AC Cord	7.5A 2.5m	電源コード	A
**	VH890400	AC Cord	6A 2.5m	電源コード	B
**	XG620A00	Power Transformer		電源トランス	J
**	XG621A00	Power Transformer		電源トランス	U,C
**	XG622A00	Power Transformer		電源トランス	H,D,A,B

* New Parts (新規部品)

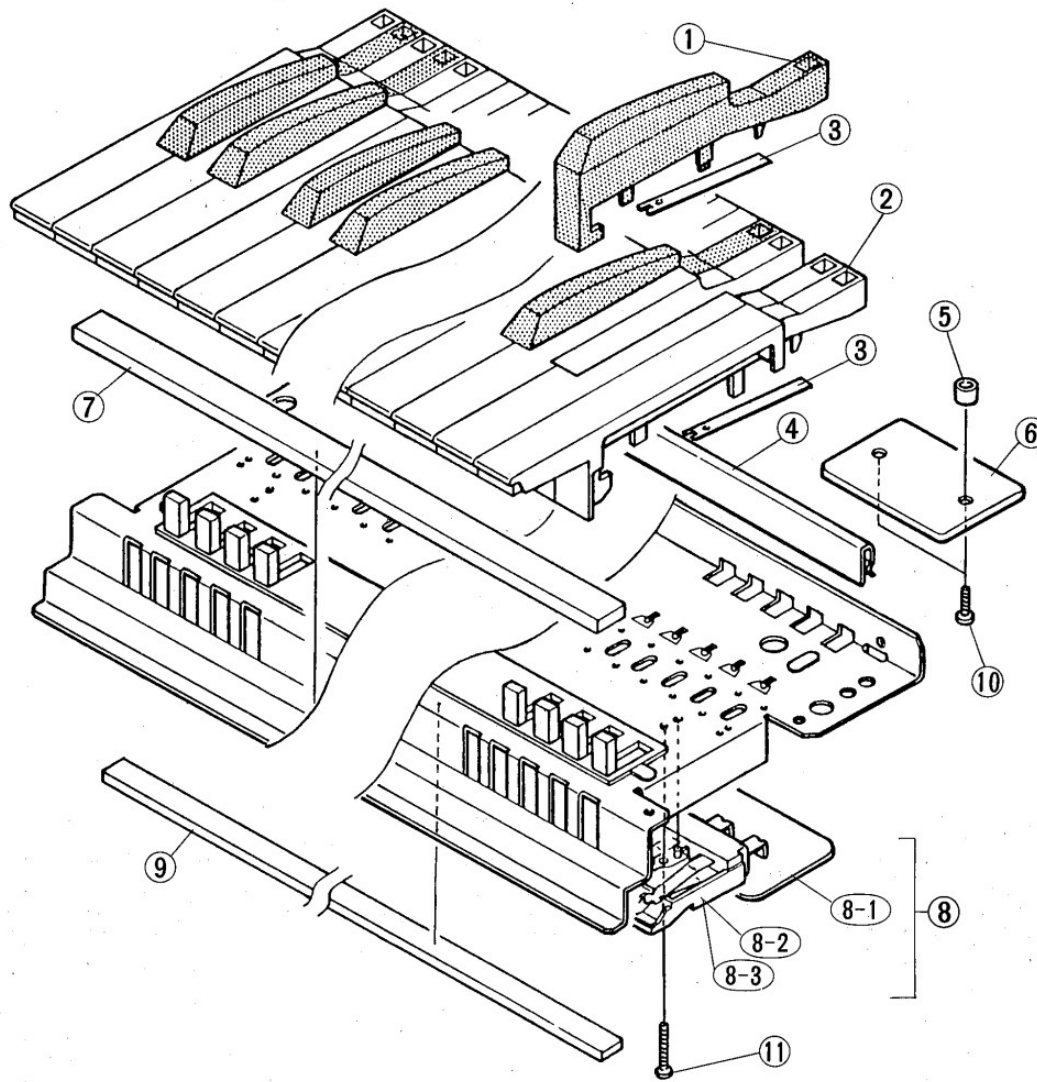
ランク: Japan only

OVERALL ASSEMBLY (総組立)



Ref. No.	Part No.	Description	部品名	Remarks	ランク
1	VH809100	Control Panel	コントロールパネル		25
2	VB774000	Knob	ツマミ	VOLUME, D.ENTRY	01
3	VH810000	Escutcheon, Slide Volume	スライトボリュームエスカッション		02
4	VH810200	Dust Proof Cloth-2	防塵クロス(2)		01
5	VH812800	Card Guide	カードガイド		06
6	NX808430	Circuit Board	CARD	CARDシート	
7	VH811500	Function Keys	SHIFT,F1-8,EXIT	ファンクションキー	03
8	VI250800	Rotary Knob	(×3)	ロータリーツマミ	01
9	VH810400	Knob-A	(×8)	ノブA(8連)	02
10	VI524400	Knob-B	(×3) 7,8,9	ノブB(3連)	02
11	VI524500	Knob-C	(×3) 4,5,6	ノブC(3連)	02
12	VI524600	Knob-D	(×3) 1,2,3	ノブD(3連)	02
13	VI524700	Knob-E	(×3) 0,-,ENTER	ノブE(3連)	02
14	VI524300	Knob-G	(×3)	ノブG(3連)	01
15	VI534600	Knob-H	(×3) ↑(center)	ノブH(3連)	03
16	VI537200	Knob-I	(×3) ←,↓,→	ノブI(3連)	03
17	VH810500	Knob-J	(×4)	ノブJ(4連)	01
18	VH810600	Knob-K	(×3)	ノブK(3連)	01
19	VH811600	LCD Filter		保護板	06
20	VH811400	Escutcheon, LCD		LCDエスカッション	05
21	VF931200	LCD	DMF-5005H	液晶ディスプレイ	28
22	VH799200	Circuit Board	PNAB	P N A B シート	
23	VH810100	Dust Proof Cloth-1		防塵クロス(1)	01
24	VH799400	Circuit Board	PNC	P N C シート	
25	VI742200	Shield Sheet		シールドシート	03
26	NX808420	Circuit Board	JKAN	J K A N シート	
27	VH810700	Angle Bracket	Center	センターアングル	08
28	VH809500	End Block	Left	拍子木(左)	09
29	VH809900	Side Board	Left	側板(左)	04
30	VH809700	Shield Plate	Left	シールド板(左)	07
31	VI625800	Wheel Assembly		ホイール Ass'y	
32	VG782900	Floppy Disk Drive Unit	D357B 3.5inch	F D D ライブユニット	26
33	VH813000	Angle Bracket, FDD		F D D 金具	04
34	VI572100	Keyboard Assembly	FS C61	鍵盤 Ass'y	36
35	VH809200	End Block	Right	拍子木(右)	07
36	VH809600	Shield Cover	Right	シールド板(右)	05
37	VH809800	Side Board	Right	側板(右)	04
38	VH810900	Angle Bracket-L, Earth		アースアングル(L)	05
39	VI474900	Angle Bracket-S, Earth		アースアングル(S)	01
40	XG620A00	Power Transformer		電源トランス	J
40	XG621A00	Power Transformer		電源トランス	U, C
40	XG622A00	Power Transformer		電源トランス	H, D, A, B
41	VD279200	AC Cord	7A 2.5m	電源コード	J
41	VD279400	AC Cord	10A 2.5m	電源コード	U
41	VD279500	AC Cord	10A 2.5m	電源コード	C
41	VD280400	AC Cord	2.5A 2.5m	電源コード	H, D
41	VD279700	AC Cord	7.5A 2.5m	電源コード	A
41	VH890400	AC Cord	6A 2.5m	電源コード	B
42	CB811230	Cord Strain Relief	SR-6N-4	コードストッパー	U
42	CB806850	Cord Strain Relief	SR-6N3-4	コードストッパー	C
42	CB072750	Cord Strain Relief	SR-4N-4	コードストッパー	H, D, B
42	CB032840	Cord Strain Relief	SR-5N-4	コードストッパー	A
43	VH812600	AC Panel		A C パネル	J
43	VI319500	AC Panel		A C パネル	U
43	VI319600	AC Panel		A C パネル	C
43	VI319700	AC Panel		A C パネル	H, D, A, B
44	CB825380	Push Button		プッシュボタン	POWER
45	VH799600	Circuit Board	PS	P S シート	J
45	VH799700	Circuit Board	PS	P S シート	U, C
45	VH799800	Circuit Board	PS	P S シート	H, D, A, B
46	VI580000	Insulation Sheet, AD		A D 絶縁シート	C
47	VH799100	Circuit Board	DM2	D M 2 シート	
48	VH799000	Circuit Board	DM1	D M 1 シート	
49	VI648000	Bottom Cover Assembly		底板 Ass'y	15
49-1	VC999400	Foot	205Y4179	ゴム足	01
50	E1330066	Bind Head Screw	3.0×6 FCM3BL	バインド小ネジ	01
51	E1330086	Bind Head Tapping Screw	3.0×8 FCM3BL	ハインドタッピングネジ	01
52	E1340106	Bind Head Tapping Screw	4.0×10 FCM3BL	ハインドタッピングネジ	01
53	E1340166	Bind Head Tapping Screw	4.0×16 FCM3BL	ハインドタッピングネジ	01
54	E2000460	Bonding Tapping Screw	3.0×8 FCM3BL	ボンディングタッピングネジ	01
55	VI491300	Bonding Tapping Screw	4.0×10 FCM3BL	ボンディングタッピングネジ	
56	EV413036	Toothed Lock Washer	A φ 3.0 FCM3BL	歯付座金内歯形	01
		* ACCESSORIES		* 付属品	
	XH062A00	Floppy Disk Floppy Disk Plug Cover	Demo. disk-B 3.5inch 1M 200X300	書込済みFD(B) フロッピーディスク プラグカバー	J U, C, H, D, A, B

KEYBOARD ASSEMBLY (鍵盤Ass'y)



Ref. No.	Part No.	Description		部品名	Remarks	ランク
*	V1572100	Keyboard Assembly	FS C61	鍵盤 Ass'y		36
1	NB107600	Black Key Assembly		黒鍵 Ass'y		03
2	NB107540	White Key Assembly	C, F	白鍵 Ass'y		03
2	NB107550	White Key Assembly	D	白鍵 Ass'y		03
2	NB107560	White Key Assembly	B, E	白鍵 Ass'y		03
2	NB107570	White Key Assembly	G	白鍵 Ass'y		03
2	NB107580	White Key Assembly	A	白鍵 Ass'y		03
2	NB107590	White Key Assembly	C'	白鍵 Ass'y		03
3	AA055430	Key Spring		鍵パネ		02
4	CB045760	Stopper		ストッパー		02
5	EZ000460	Spacer	#00374 4.0×5	スペーサー		01
6	NA109720	Circuit Board	PC	PCセンサー		07
7	PB000470	PC Sensor	(L)	PCセンサー		16
8	NB116200	Key Switch Unit	FS	MKスイッチユニット		19
8-1	NA115670	Circuit Board	MK	MKシート		09
8-2	NB107120	Key Switch Assembly	12Q FS	スイッチ Ass'y		08
8-3	NB107110	Key Switch Assembly	13K FS	スイッチ Ass'y		08
9	CC030570	Felt	821×6×3 WH	フェルト(白)		03
10	ED330106	Bind Head Screw	3.0×10 FCM3BL	バインド小ネジ		01
11	ED330166	Bind Head Screw	3.0×16 FCM3BL	バインド小ネジ		01

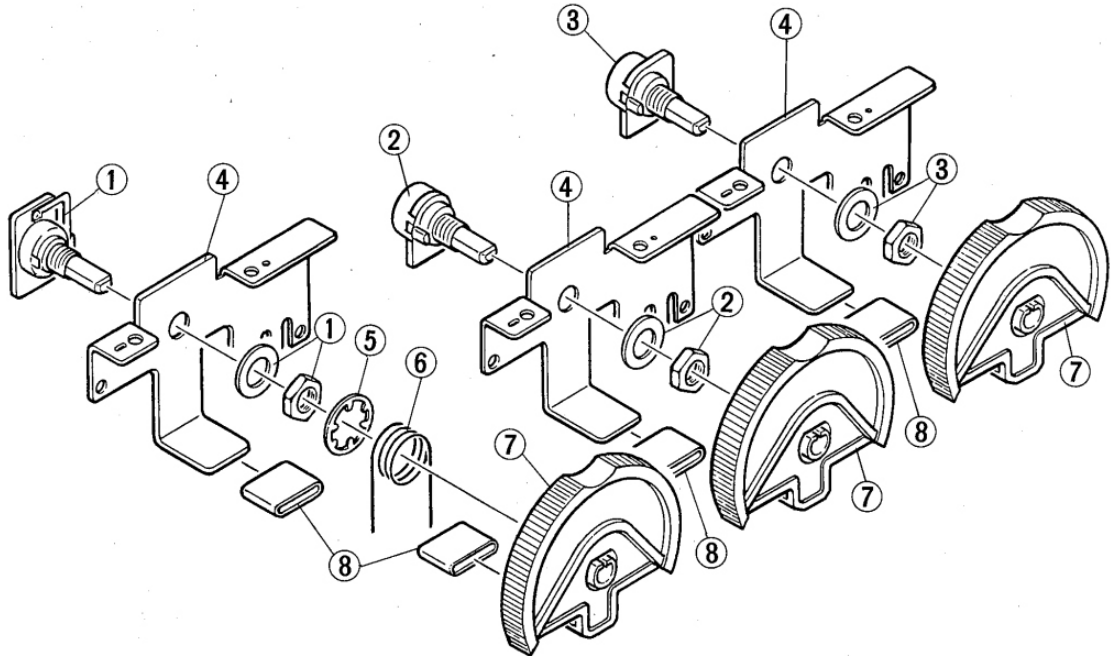
* New Parts (新規部品)

ランク: Japan only

SY77

■ WHEEL ASSEMBLY (ホイールAss'y)

SY77



Ref. No.	Part No.	Description	部品名	Remarks	ランク
*	VI625800	Wheel Assembly	ホイール Ass'y		
1	VE469300	Variable Resistor	ロータリーポリウム	PITCH BEND	03
2	NS412160	Variable Resistor	ロータリーポリウム	MODULATION 1	03
3	VI668700	Variable Resistor	ロータリーポリウム	MODULATION 2	03
4	VF536800	Frame	フレーム		01
5	EW600110	Wheel Ring	C S 形 止め輪	PITCH BEND	01
6	VC792800	Spring	リターン スプリング	PITCH BEND	01
7	VF537400	Wheel	ホイール		02
8	CB819020	Wheel Tube	ホイールチューブ		02

* New Parts (新規部品)

ランク : Japan only