μA726

TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA726 is a monolithic transistor pair in high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling, and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift DC amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process.

ABSOLUTE MAXIMUM RATINGS

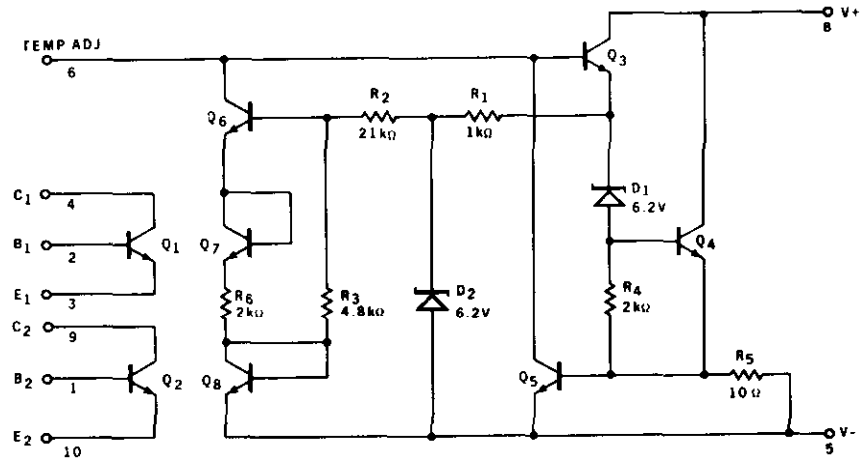
Operating Temperature Range	
Military (312 Grade)	−55°C to +125°C
Commercial (323 Grade)	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C
Supply Voltage	±18 V
Internal Power Dissipation	500 mW

MAXIMUM RATINGS FOR EACH TRANSISTOR

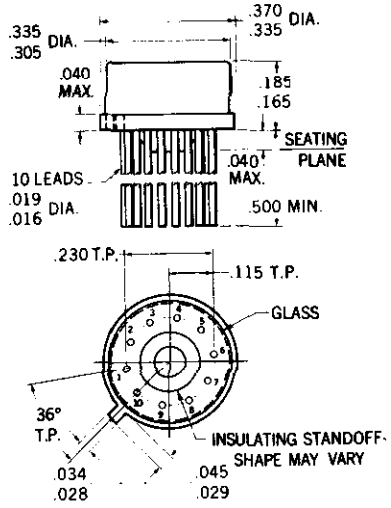
Maximum collector-to-substrate voltage	40 V
BV_{CBO}	40 V
LV_{CEO} (Note 1)	30 V
BV_{EBO}	5 V
Collector Current	5 mA

Note 1: Measured at 1 mA collector current.

SCHEMATIC DIAGRAM



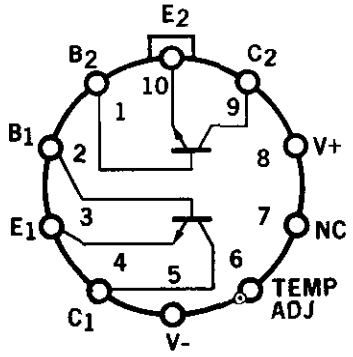
PHYSICAL DIMENSIONS



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

ORDER PART NOS. U5U7726312
U5U7726323

CONNECTION DIAGRAM
(TOP VIEW)



*Planar is a patented Fairchild process

312 GRADE

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_S = \pm 15$ V, $R_{adj} = 62$ kΩ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	10 μA ≤ I_C ≤ 100 μA V_{CE} = 5 V, R_S ≤ 50Ω		1.0	2.5	mV
Input Offset Current	I_C = 10 μA, V_{CE} = 5 V		10	50	nA
Input Offset Current	I_C = 100 μA, V_{CE} = 5 V		50	200	nA
Average Input Bias Current	I_C = 10 μA, V_{CE} = 5 V		50	150	nA
Average Input Bias Current	I_C = 100 μA, V_{CE} = 5 V		250	500	nA
Offset Voltage Change	I_C = 10 μA, 5 V ≤ V_{CE} ≤ 25 V, R_S ≤ 100 kΩ		0.3	6.0	mV
Offset Voltage Change	I_C = 100 μA, 5 V ≤ V_{CE} ≤ 25 V, R_S ≤ 10 kΩ		0.3	6.0	mV
Input Offset Voltage Drift	10 μA ≤ I_C ≤ 100 μA, V_{CE} = 5 V, R_S ≤ 50Ω, +25°C ≤ T_A ≤ +125°C		0.2	1.0	μV/°C
Input Offset Voltage Drift	10μA ≤ I_C ≤ 100 μA, V_{CE} = 5 V, R_S ≤ 50Ω, −55°C ≤ T_A ≤ +25°C		0.2	1.0	μV/°C
Input Offset Current Drift	I_C = 10 μA, V_{CE} = 5 V		10		pA/°C
Input Offset Current Drift	I_C = 100 μA, V_{CE} = 5 V		30		pA/°C
Supply Voltage Rejection Ratio	10μA ≤ I_C ≤100 μA, R_S ≤ 50Ω,		25		μV/V
Low-Frequency Noise	I_C = 10 μA, V_{CE} = 5 V, R_S ≤ 50Ω BW = .001 Hz to 0.1 Hz		4.0		μV pp
Broadband Noise	I_C = 10 μA, V_{CE} = 5 V, R_S ≤ 50Ω BW = 0.1 Hz to 10 kHz		10		μV pp
Long-term Drift	10 μA ≤ I_C ≤ 100 μA, V_{CE} = 5 V, R_S ≤ 50Ω, T_A=25°C		5.0		μV/week
High Frequency Current Gain	f = 20 MHz, I_C = 100 μA, V_{CE} = 5 V	1.5	3.5		
Output Capacitance	I_E = 0, V_{CB} = 5 V		1.0		pF
Emitter Transition Capacitance	I_E = 100 μA		1.0		pF
Collector Saturation Voltage	I_B = 100 μA, I_C = 1 mA		0.5	1.0	V

323 GRADE

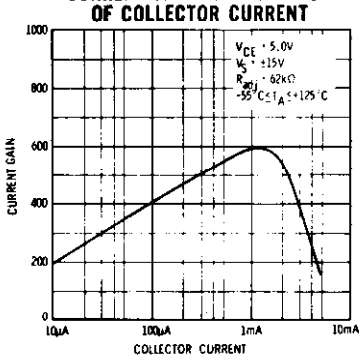
ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +85°C$, $V_S = \pm 15$V, $R_{adj} = 75$ kΩ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	10 μA ≤ I_C ≤ 100 μA V_{CE} = 5V, R_S ≤ 50Ω		1.0	3.0	mV
Input Offset Current	I_C = 10 μA, V_{CE} = 5V		10	100	nA
Input Offset Current	I_C = 100 μA, V_{CE} = 5V		50	400	nA
Average Input Bias Current	I_C = 10 μA, V_{CE} = 5V		50	300	nA
Average Input Bias Current	I_C = 100 μA, V_{CE} = 5V		250	1000	nA
Offset Voltage Change	I_C = 10 μA, 5V ≤ V_{CE} ≤ 25V, R_S ≤ 100 kΩ		0.3	6.0	mV
Offset Voltage Change	I_C = 100 μA, 5V ≤ V_{CE} ≤ 25V, R_S ≤ 10 kΩ		0.3	6.0	mV
Input Offset Voltage Drift	I_C = 100 μA, V_{CE} = 5V, R_S ≤ 50Ω		0.2	2.0	μV/°C
Input Offset Current Drift	I_C = 10 μA, V_{CE} = 5V		10		pA/°C
Input Offset Current Drift	I_C = 100 μA, V_{CE} = 5V		30		pA/°C
Supply Voltage Rejection Ratio	I_C = 100 μA, R_S = 50Ω		25		μV/V
Low-Frequency Noise	I_C = 10 μA, V_{CE} = 5V, R_S ≤ 50Ω, BW = 0.001 Hz to 0.1 Hz		4.0		μV pp
Broadband Noise	I_C = 10 μA, V_{CE} = 5V, R_S ≤ 50Ω, BW = 0.1 Hz to 10 kHz		10		μV pp
Long-Term Drift	I_C = 100 μA, V_{CE} = 5V, R_S ≤ 50Ω, T_A = 25°C		5.0		μV/week
High-Frequency Current Gain	f = 20 MHz, I_C = 100 μA, V_{CE} = 5V	1.5	3.5		
Output Capacitance	I_E = 0, V_{CB} = 5V		1.0		pF
Emitter Transition Capacitance	I_E = 100 μA		1.0		pF
Collector Saturation Voltage	I_B = 100 μA, I_C = 1 mA		0.5	1.0	V

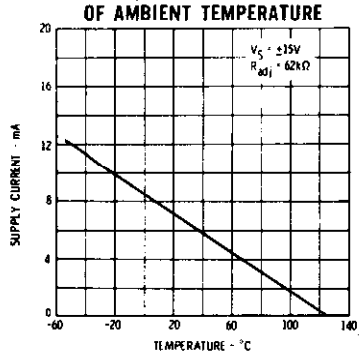
TYPICAL PERFORMANCE CURVES

312 GRADE

CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT

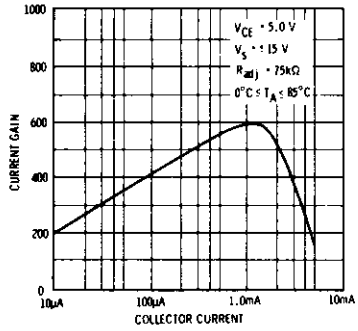


SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

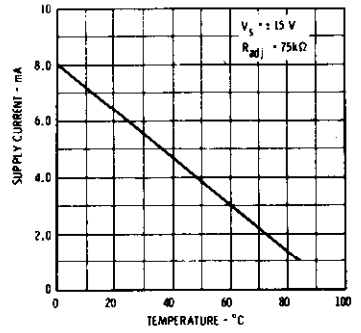


323 GRADE

CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL X1000 CIRCUIT